ECE 327: *Electronic Devices and Circuits Laboratory I*

Notes for Lab 6 (Digital-to-Analog Converter (DAC) Lab)

1. Strictly speaking, **this laboratory is *not* about digital-to-analog conversion**.
   - A DAC converts an *abstract numerical* quantity to a physical quantity (e.g., a voltage)
   - "Current-summing" DAC uses binary-weighted currents — switches select which currents to sum
     - In practice, single-pole *double*-throw (SPDT) switches are used (i.e., no "floating")
     - Can generate currents with binary-weighted resistors
       - Turning on and off currents quickly causes switching transients (i.e., introduces noise)
       - Instead, switch *constant* current flow toward and away from sum junction
       - Binary-weighted resistors are difficult to implement (especially for high number of bits)
     - R–$2R$ ladder — used to make a more clever current-summing DAC (Figure L6-1)
       - Need R, $2R$, and switch per bit
         - Much easier to match R and $2R$ (helps with linearity — refer to INL and DNL)
       - DAC input impedance is $2R$ regardless of number of bits and switch states
         - Each new bit just splits off more current
         - Constant current means no switching transients
     - Multiplier DAC (mDAC) — *like* a "digital potentiometer"
       - *Ratiometric*: Output is a ratio of input (usually power supply)
         - Principle used in relaxation oscillators to make them insensitive to power supply changes
         - Frequently used with sensors for same purpose
     - Use zero-order hold (ZOH) to construct analog signal from digital time series
       - Result is **pulse-amplitude modulated (PAM)** version of digital signal
       - Low-pass filter to smooth edges if necessary (sometimes system is enough of a filter)
         - "Oversampling" can increase filter performance and decrease its complexity and *cost*
         - "Oversampling": reconstructing a time series at much higher frequency by interpolation
   - Alternative: "Oversample" and use **"1-bit DAC"** (looks sexy on shiny metallic label)
     - "1-bit DAC": Each point is represented as one of two analog states (*cheap* to implement)
     - Filtering the quickly switching output produces the desired analog signal
     - Marketers make empty/nonsensical claims of *quantization noise* reduction (real benefit: *cost*)
     - **Pulse-density modulation (PDM, Σ-Δ, Δ-Σ, SDM)** is frequently used
       - Simple low-pass filter (LPF) restores analog signal
       - LPF can be omitted if load has appropriate frequency response
   - Pulses are often used in digital communication
     - **pulse-code modulation (PCM)** represents binary **c**odes as serial high and low **p**ulses
       - e.g., compact disc digital audio (CDDA) — "pit"-"land" *transitions* encode "1"
       - a sequence of pulses (e.g., 7 subsequent pulses) represents one "code"
       - error-correction methods exist (e.g., redundancy)
       - can multiplex (MUX) in time (e.g., stereo — left and right channels)
   - Pulses are not strictly digital — can store *analog* information in *time*

2. Pulse modulation and amplifier efficiency

- Amplifier types (i.e., "classes") — From least to most efficient
  - Class A
    - All devices (e.g., transistors) are in *active* mode
      - e.g., power supplied from *both* rails at *all* times and dissipated through transistors
    - Devices **dissipate** power to replicate signal *exactly* (i.e., to place output **between** rails)
    - High-fidelity but high power loss and bulky components
    - Maximum 50% efficiency (i.e., equal power dissipated in amplifier as in load)
  - Class B
    - Devices move into *cutoff mode* for half of a sine wave input cycle
      - e.g., power supplied from only *one supply rail* at a time
    - Distortion from switching from active to cutoff modes
    - Maximum 78.5% (i.e., $\pi/4$) efficiency
  - Class C
    - Like class B, but in *cutoff* for even longer (i.e., *extremely* high distortion)
      - Visualize one **impulse** for every input cycle
      - *Extremely* efficient (very little amplifier conduction, so 80% or higher efficiency)
    - Loads are tuned (e.g., high-Q *LC* filter) for narrow bandwidth applications (e.g., RF)
      - Like hitting a bell with a hammer
      - Load "rings" at desired frequency
      - Information theory connection: narrow bandwidth implies high prior information
  - Class D (and trademarked variations of the "switching amplifier")
    - Devices are *never* active — they act like **SWITCHES**
      - Switches don't dissipate power ($i = 0$ or $v = 0$, so $i \times v = 0$)
      - Contrast with dissipative "active" "dimmers"
      - Efficiencies in 90% neighborhood and components are cheap and small
    - Input signal is modulated over output pulses
      - Pulse-width (PWM) or Pulse-density modulation (PDM) are frequently used
      - More exotic models use "sliding mode" tracking (OSU ECE's Utkin, Lenin prize)
      - "H-bridge" (Figure L6-2) — positive, negative, zero (braking), and floating output
      - High-efficiency LC filter can be used to smooth output if necessary
    - Amplification by switching between supply rails — no active components needed
      - Voltage gain through switching high voltage rails
      - Power gain by switching rails capable of high current
    - Our PWM **modem** can be viewed as a class-D amplifier
      - To double received signal, design receiver for 20 V rail
    - **Switching** amplifiers and converters are major subjects of ECE 624/628/720/724

3. Typical demodulation of PWM

- PWM and PDM look like modulated signal near DC (i.e., "average" of pulses tracks signal)
  - Demodulation *eventually* extracts baseband signal with "filter"
  - Nonlinear preconditioning concentrates baseband and removes lower sampling harmonics
- "Natural sampling" with sawtooth or can be demodulated with LPF alone
  - Pulse widths are too small for hysteresis requirements of our infrared (IR) receiver.
- "Uniform sampling" is sampled, and so it requires conversion to PAM first

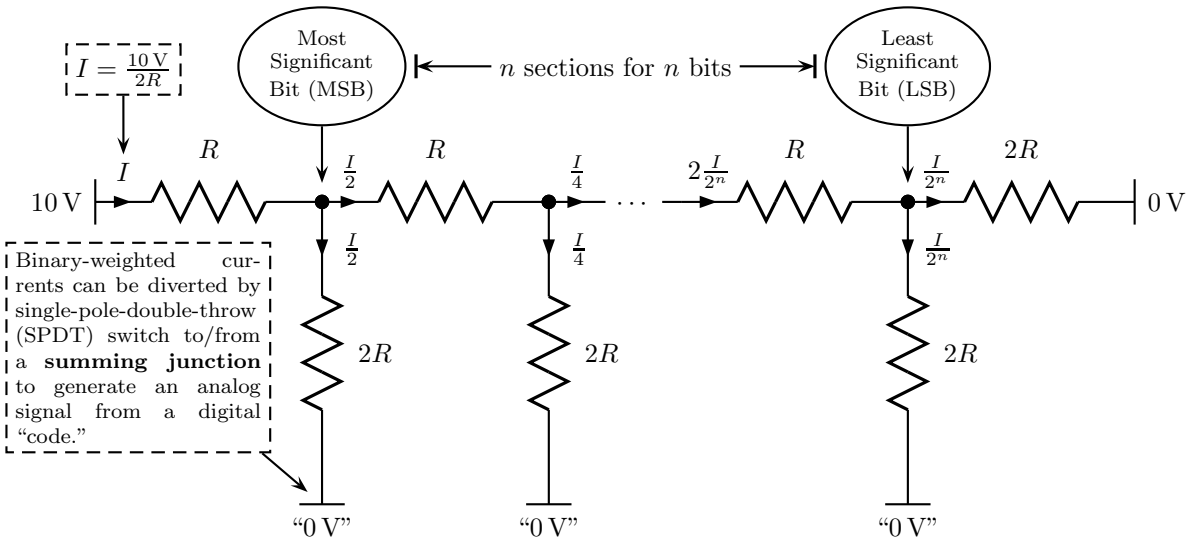

Figure L6-1: "R–$2R$ ladder" for current-summing digital-to-analog converter (DAC). Circuit is easy to implement and does not cause switching transients when input "code" is changed. Input impedance is $2R$, and so total current through ladder is $(10\,\text{V})/(2R)$ regardless of number of wrungs and switch states. Current through each $2R$ "wrung" of "ladder" is half of current in previous wrung. So the currents in the wrungs are binary-weighted. Each 0 V connection can be selectively switched from "real ground" to a "virtual ground." The selected currents at the virtual ground will sum, and the resulting current will be an analog version of the digital input (i.e., the switch states).

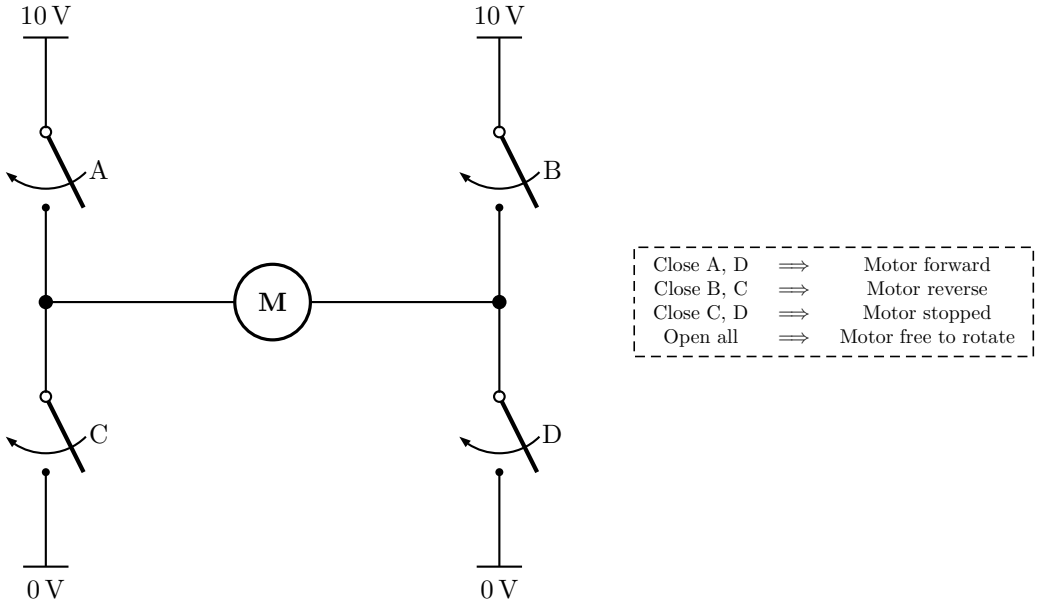

Figure L6-2: "H-bridge" for driving smooth loads with discrete output. Circuit can be used with a 1-bit output to drive a motor (or other load) forwards *or backwards*. Additionally, output can be switched to float (e.g., a free-spinning motor) or be shorted (e.g., for primitive "dynamic braking" of a motor). Moving *quickly* between states (e.g., forward to stop to forward again) forces the load into some intermediate behavior, and so smooth outputs are possible from discrete controls.

4. Demodulation of PWM in the lab — *similar* to "uniform sampling"
   (i) Integrate pulse to get a *new* ramp, and then reset — result is like a sawtooth
   (ii) Sample and hold (switch, capacitor, buffer) ramps just before reset — hills, plateaus, and cliffs
   (iii) Sample and hold again to remove hills — PAM result
   (iv) Filter PAM through low-pass filter to smooth signal

   Circuits (ii) and (iii) are "analog D flip–flop" (i.e., master–slave "latch"): samples ramp at pulse edge

5. Infrared (IR) receiver: built-in "debouncing" circuit
   - A "raw" infrared receiver is noisy and insensitive
   - Increased gain increases sensitivity — output is either high or low but false positives are frequent
   - Use RC "slowdown" network (demodulation) and Schmitt trigger hysteresis (thresholds)
     - "Slowdown" network and triggering imposes limit on smallest pulse width (6 μs in our case)
     - Minimum pulse width makes "natural sampling" PWM method impossible

6. Parts in the lab
   - Use QEE113 infrared transmitter (*not* the MLED930)
     - Build driver as shown in supplementary text
     - *pnp* drivers are "active low" — use $\overline{Q}$ instead of Q if you use one of these
     - Infrared light is *invisible* — you **will not see it**
   - Use QSE157 infrared receiver (*not* the MRD5009) with built-in debouncing circuit
     - Do **not** use a pull-up resistor on output
   - Use CD4049 for 2 inverters (test before use)
   - Use CD4066 for 3 switches (test before use)
   - Use low-leakage BiMOS (MOS input, BJT gain, CMOS push–pull output) CA3160 operational amplifiers (for buffers)
     - If none available, use CA3130 with 45–100 pF (e.g., 68 pF) from pin 1 to pin 8 for frequency compensation (i.e., for stability of the unity-gain feedback system)
   - Capacitors:
     - Ramp generator ($C1$): Probably 2.2 nF (whatever was used in ADC lab)
     - Sample and hold ($C2$ and $C3$): 100 pF (why so small?)

7. Laboratory experience
   - Many design alternatives given
   - **Use same ramp slope as in ADC lab** — the two ramps must match
   - Make use of **bypass capacitors** at *supply pins* to reduce output noise
   - When taking plots, save as CSV or BMP
     - Saving as BMP prevents extra work, but make sure scope plots show all required information
       * Intervals between horizontal and vertical divisions should be clear
       * In most cases, channel grounds should be shown
       * Channels should be labeled in report (e.g., "top waveform is input")
     - For CSV: Label axes, show units, and identify waveforms (e.g., "input" and "output")
   - Handouts give pin-outs and detailed instructions (see book when writing report)
   - Keep resulting **PWM demodulator** for future labs

8. Laboratory reports
   - Answer all questions and provide all plots from lab procedures in lab text
   - Include ALL PLOTS from procedure (even if not mentioned in book) and USE in discussion
   - Consider answering some of the questions from the procedure