Single-Rail Level-Shifter Amplifiers

Lab 5: Analog-to-Digital Conversion

ECE 327: *Electronic Devices and Circuits Laboratory I*

Abstract

For the analog-to-digital conversion lab (and others), we need to implement a level-shifter amplifier that uses 10 V and 0 V as its power rails (i.e., a *single-ended* power supply). In this document, we explore an operational amplifier approach as well as a common-emitter NPN transistor amplifier approach to the amplifier design.

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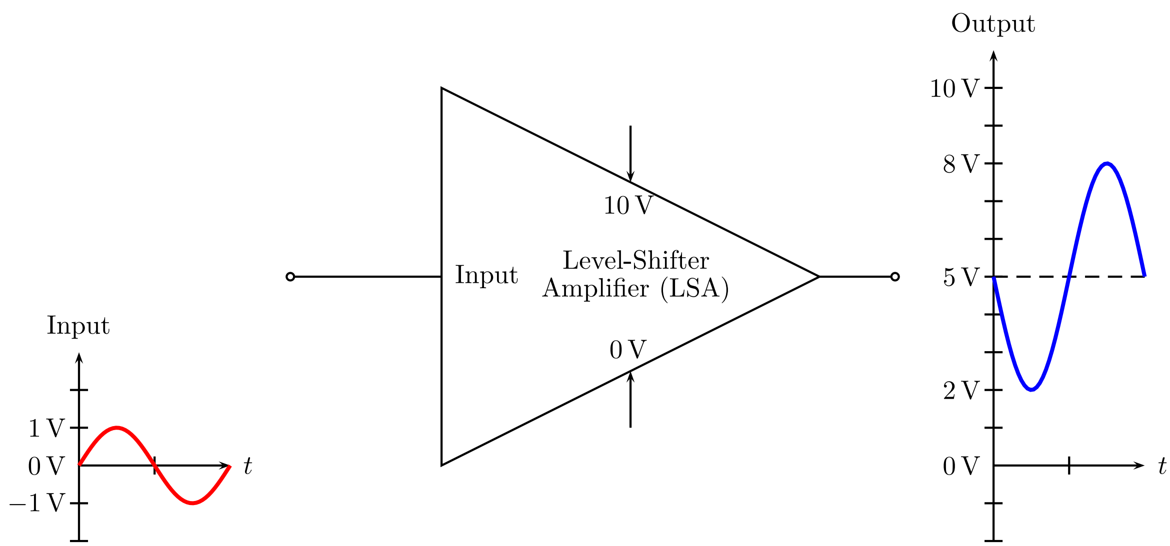
1 Introduction

Our goal is to build a circuit that takes a 2 V peak-to-peak signal centered at 0 V as input and translates it to a 6 V peak-to-peak signal centered at 5 V on its output. That is, we want a component like



The signals available to us are 10 V and 0 V. The input signal exists within a −1–1 V envelope. The output signal must be a (possibly inverted) version of the input signal that exists within a 2–8 V envelope. Therefore, the *magnitude* of the amplifier gain should be 3 and the amount of DC shift should be 5 V.

Here, we investigate two different methods of implementing the level-shifter amplifier (LSA). The first uses an operational amplifier. The second, a so-called common-emitter amplifier, uses an NPN transistor. Because we desire single-ended designs, in both cases the signal input will be AC coupled to the amplifier. Lab part pin-outs are given in Appendix A.

2 Operational Amplifier LSA

In the configuration in Figure 2.1, an LM741 OA is recommended, but an LF351 may be used instead.

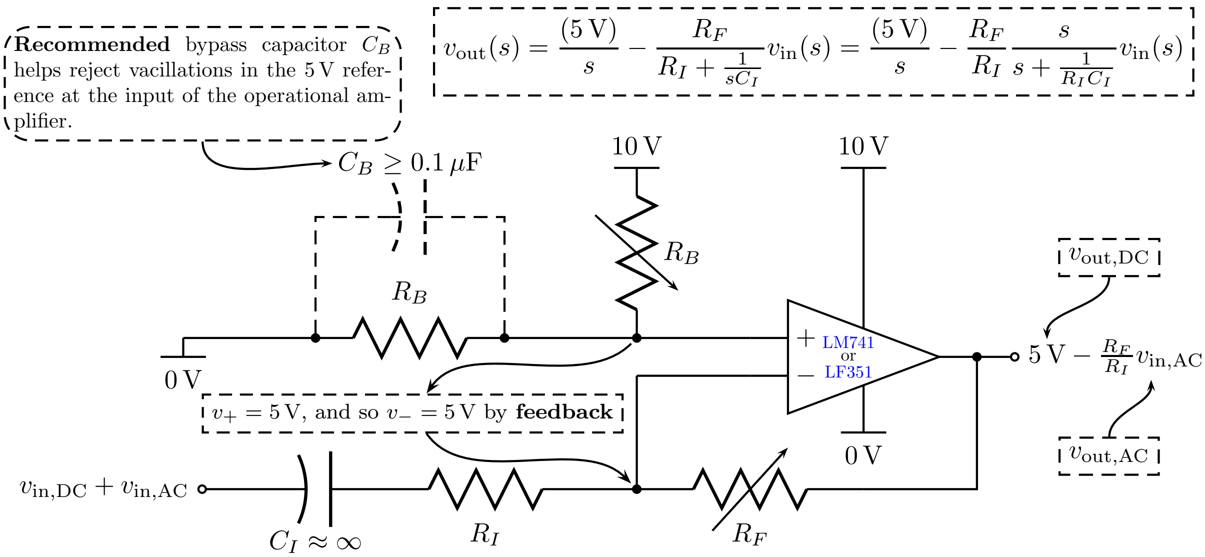


Figure 2.1: Single-ended level-shifter amplifier implemented with operational amplifier.

The capacitor C_I is an open circuit (i.e., ∞ impedance) to DC, and so no DC current flows through R_I or R_F. Therefore, the output of the amplifier naturally has a 5 V DC component (i.e., the output is automatically shifted). So the components R_F and R_I must be chosen to give the appropriate AC gain and C_I must be chosen large enough to pass signals of interest. Use the method of superposition to verify this analysis.

Assume that C_I is a short-circuit to signals of interest (i.e., it has low impedance compared to R_I for input signal frequencies). To provide a gain of 3 to these signals, R_F and R_I must be chosen so that

$$\frac{R_F}{R_I} = 3, \qquad \text{which means} \qquad R_F = 3R_I \qquad \text{and} \qquad R_I = 0.25 \times \underbrace{(R_I + R_F)}_{\text{potentiometer total}}. \tag{2.1}$$

Using a potentiometer for the R_I–R_F divider, choose components[1] so that

$$C_I \leq 2\,\mu\text{F} \qquad \text{and} \qquad \frac{1}{2\pi R_I C_I} \leq 35\,\text{Hz} \qquad \text{and} \qquad 10\,\text{k}\Omega \leq R_F \leq 50\,\text{k}\Omega. \tag{2.2}$$

Use the R_I–R_F potentiometer to **tune the gain**. After tuning the gain, **be sure your half-power frequency** is *no higher* than 35 Hz and increase C_I if needed.

The output DC offset is set with the R_B–R_B divider, which **should be implemented with a potentiometer**. Use the R_B–R_B potentiometer to **tune the offset**. **If you can**, ensure that[2]

$$R_B \approx 2R_F \qquad \text{and} \qquad 1\,\text{k}\Omega \leq R_B \leq 500\,\text{k}\Omega \tag{2.3}$$

for good high frequency performance, low current draw, and high robustness to device variations.

Polarized capacitors: In our lab, large capacitors are only available as polarized electrolytic capacitors. Keep capacitors small so that polarized capacitors are not needed, and **use small capacitors in parallel** to implement large capacitances. If you *need* a polarized capacitor, **it must be wired so that** its cathode (i.e., the "negative" end of the capacitor, which is drawn as a curved line) sees a lower DC potential than its anode[3]. Because our input has negligible DC component and our shifted output has a 5 V DC component, C_I should be wired with its cathode (i.e., "negative" end) toward the input, as shown in Figure 2.1.

[1] Try starting with potentiometer *total* $R_I + R_F \geq 20\,\text{k}\Omega$ and $C_I \geq 0.47\,\mu$F.
[2] Try starting with potentiometer total $R_B + R_B \geq 50\,\text{k}\Omega$ (and $C_B \geq 0.1\,\mu$F).
[3] Remember that **A**node **C**urrent **E**nters (ACE), **C**athode **C**urrent **D**eparts (CCD), and **C**athodes are **C**urved.

3 NPN Common-Emitter LSA

Both NPN and PNP[4] common-emitter amplifiers are naturally LSAs. Here, we focus on the NPN case. The same approach could be applied to designing a PNP common-emitter LSA.

In the first example below, the standard common-emitter configuration leads to output "clipping" from transistor saturation. This flaw motivates the second example, which attenuates the input and increases the common-emitter amplification in order to avoid transistor saturation. Both examples are single-ended (i.e., they only use 10 V and 0 V for power rails).

Bad LSA: Full-scale input case

Consider Figure 3.1 for some $t \geq 0$.

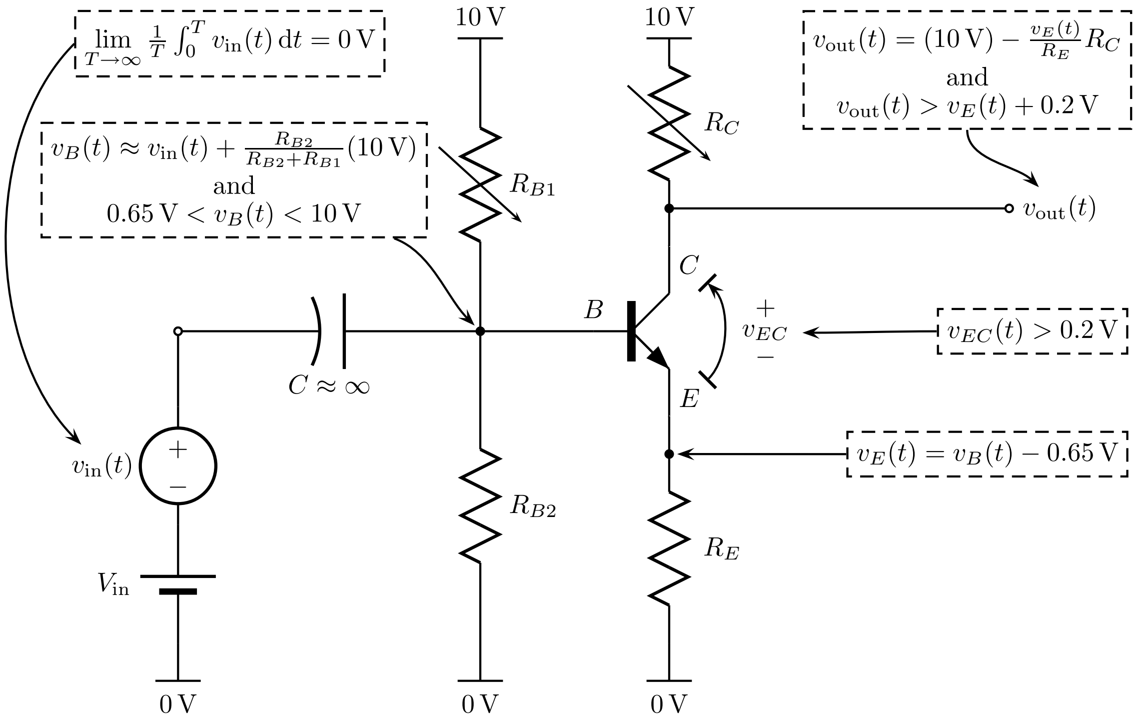


Figure 3.1: Level-shifter amplifier implemented with single-ended common-emitter NPN configuration.

The input is composed of a DC (i.e., average) part V_{in} and a purely AC (i.e., zero average) part v_{in}. The capacitor C_I is meant to AC couple the signal to the base of the transistor. That is, it should be chosen so large that it is a short-circuit to all frequencies of interest. We will give guidelines for choosing C_I later; for the moment, assume that it passes v_{in} and blocks V_{in}.

First, we need to pick the values of R_E, R_C, R_{B2}, and R_{B1} to give us v_{in} gain magnitude of 3 and DC offset of 5 V. We want to assume that the transistor is in active mode with negligible base current and very high current gain (i.e., $\beta \gg 0$). So we can take the value of v_{out} to be

$$\begin{aligned} v_{out}(t) &= (10\,V) - (v_B(t) - 0.65\,V)\frac{R_C}{R_E} \\ &= \underbrace{(10\,V) + (0.65\,V)\frac{R_C}{R_E} - \frac{R_C}{R_E}\frac{R_{B2}}{R_{B2}+R_{B1}}(10\,V)}_{\text{DC offset}} - \underbrace{\frac{R_C}{R_E}}_{|\text{Gain}|} v_{in}(t). \end{aligned}$$

[4] Remember: Transistor symbol is "**N**ot **P**ointing i**N**" (NPN), or it "**P**oints i**N** **P**roudly" (PNP).

Because the gain magnitude should be set to 3,

$$\frac{R_C}{R_E} = 3. \tag{3.1}$$

Therefore,

$$v_{\text{out}}(t) = \underbrace{(11.95\,\text{V}) - \frac{R_{B2}}{R_{B2} + R_{B1}}(30\,\text{V})}_{\text{DC offset}} - 3v_{\text{in}}(t).$$

Because the DC offset should be 5 V,

$$\frac{R_{B2}}{R_{B2} + R_{B1}} = \frac{6.95}{30} = \frac{139}{600} = 0.23166\cdots, \tag{3.2}$$

so the transistor base sees a DC average of ~2.316 V. To guarantee negligible transistor base current, choose resistors so that

$$R_{B1} \| R_{B2} \ll \beta R_E, \tag{3.3}$$

where $\beta \approx 100$[5]. For tuning, potentiometers and/or variable resistors should be used.

Saturation/compliance problems

This design has serious problems. From Equation (3.2),

$$v_B(t) = v_{\text{in}}(t) + \frac{69.5}{30}\,\text{V} = v_{\text{in}}(t) + 2.3166\cdots\,\text{V}.$$

The input $v_{\text{in}}(t)$ ranges from -1 V to 1 V, and so

$$1.3166\cdots\,\text{V} < v_B(t) < 3.3166\cdots\,\text{V}.$$

Because $0.65\,\text{V} < v_B(t) < 10\,\text{V}$ at all times, the transistor is always biased on. Therefore, there will not be any clipping from cutoff. However, the output signal can still be distorted by transistor saturation, and so we must make sure $v_{EC} > 0.2\,\text{V}$ at all times. The emitter potential v_E is such that

$$0.66\cdots\,\text{V} < v_E(t) < 2.66\cdots\,\text{V},$$

and, for the same range, the output v_{out} is such that

$$8\,\text{V} > v_{\text{out}}(t) > 2\,\text{V}.$$

When the input rises to 1 V, the emitter *rises* to 2.66 V and the collector (i.e., the output) *falls* to 2 V, which gives a *negative* $v_{EC} = -0.66\,\text{V}$. The collector should always be at least 0.2 V *above* the emitter for *active mode* operation, so we expect the transistor will *saturate* and the output will be distorted.

Modifying to prevent clipping

Roughly speaking, the problem with this LSA is that there is not enough "room" between the 0 V and 10 V rails. Two easy ways to solve this problem are:

(i) Provide a sufficiently negative rail (e.g., -10 V) for the common-emitter amplifier.

(ii) Attenuate the input signal so it has less peak-to-peak swing.

To keep the amplifier single-ended, we implement item (ii) for our NPN common-emitter LSA. In particular, we cut the input signal in half and double the common-emitter gain (from 3 to 6).

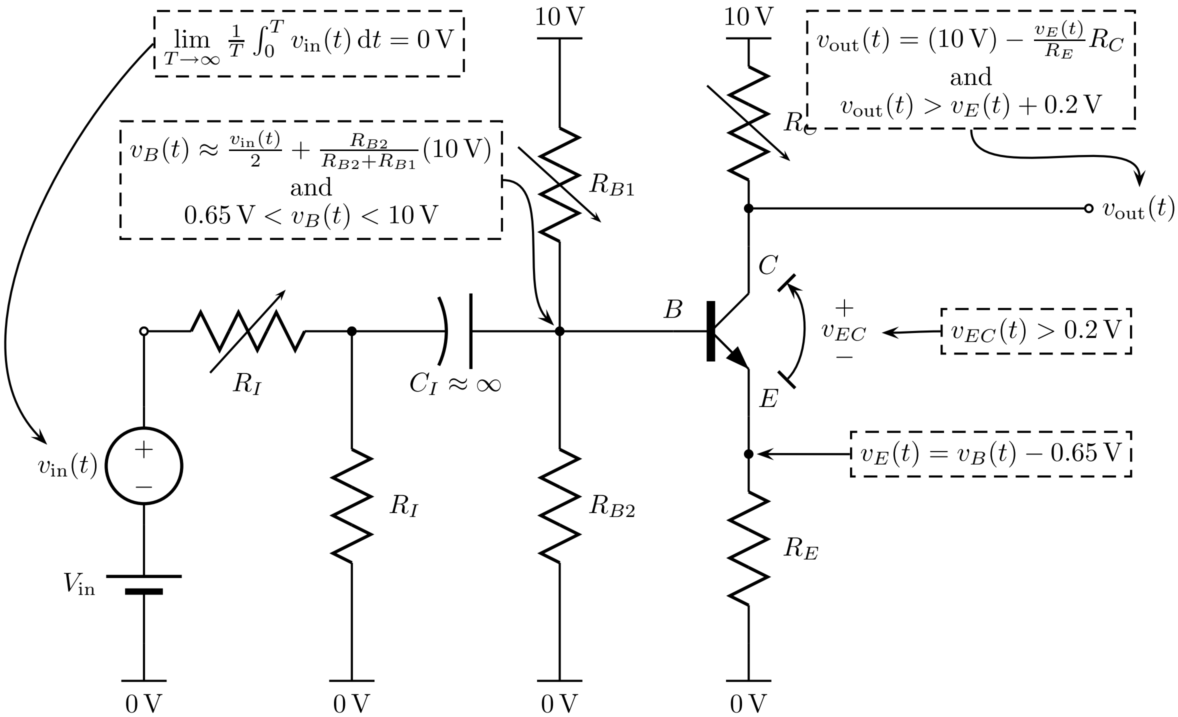


Figure 3.2: Level-shifter amplifier implemented with attenuated-input common-emitter NPN configuration.

Good LSA: Attenuated input swing

Consider Figure 3.2, which is identical to Figure 3.1 except that the input signal is attenuated before being coupled to the transistor base[6]. The circuit is easy to analyze provided that $C_I \approx \infty$ (i.e., a short-circuit for signals of interest) and

$$0 \ll R_I \| R_I \ll R_{B1} \| R_{B2} \ll \beta R_E, \tag{3.4}$$

where $\beta \approx 100$. For tuning, potentiometers and/or variable resistors should be used. The output

$$v_{\text{out}}(t) = \underbrace{(10\,\text{V}) + (0.65\,\text{V})\frac{R_C}{R_E} - \frac{R_C}{R_E}\frac{R_{B2}}{R_{B2}+R_{B1}}(10\,\text{V})}_{\text{DC offset}} - \underbrace{\frac{R_C}{R_E}\frac{1}{2}}_{|\text{Gain}|} v_{\text{in}}(t).$$

The LSA gain magnitude should be set to 3, so

$$\frac{R_C}{R_E}\frac{1}{2} = 3, \qquad \text{which means} \qquad \frac{R_C}{R_E} = 6. \tag{3.5}$$

Therefore,

$$v_{\text{out}}(t) = \underbrace{(13.9\,\text{V}) - \frac{R_{B2}}{R_{B2}+R_{B1}}(60\,\text{V})}_{\text{DC offset}} - 3v_{\text{in}}(t).$$

Because the DC offset should be 5 V,

$$\frac{R_{B2}}{R_{B2}+R_{B1}} = \frac{8.9}{60} = \frac{89}{600} = 0.14833\cdots, \tag{3.6}$$

so the transistor base sees a DC average of $\sim$1.483 V.

[5] This β-estimate is conservative for a 2N3904.
[6] Alternatively, a single $R_I = R_{B1} \| R_{B2}$ in series with v_{in} can be used *instead* of the R_I–R_I divider.

Compliance and linearity

From Equation (3.6),

$$v_B(t) = \frac{v_{\text{in}}(t)}{2} + \left(\frac{890}{600}\,\text{V}\right) = \frac{v_{\text{in}}(t)}{2} + 1.4833\cdots\,\text{V}.$$

The input $v_{\text{in}}(t)$ ranges from -1 V to 1 V, and so

$$0.9833\cdots\,\text{V} < v_B(t) < 1.9833\cdots\,\text{V}.$$

Because $0.65\,\text{V} < v_B(t) < 10\,\text{V}$ at all times, the transistor is always biased on. Therefore, there will not be any clipping from cutoff. However, the output can still be distorted by transistor saturation, and so we must make sure $v_{EC} > 0.2\,\text{V}$ at all times. The emitter potential v_E is such that

$$0.33\cdots\,\text{V} < v_E(t) < 1.33\cdots\,\text{V},$$

and, for the same range, the output v_{out} is such that

$$8\,\text{V} > v_{\text{out}}(t) > 2\,\text{V}.$$

Now, $v_{EC} > 0.66\,\text{V}$, and so the transistor is firmly in active mode (i.e., it will not saturate). This LSA should have minimal nonlinear distortion. However, because we had to attenuate the input signal and increase the common-emitter gain, we may expect poorer noise performance.

Choosing a coupling capacitor

The $v_B/(v_{\text{in}} + V_{\text{in}})$ (i.e., input-to-base) transfer function is

$$\frac{(R_{B1} \| R_{B2}) \| \beta R_E}{(R_I \| R_I) + \frac{1}{sC_I} + (R_{B1} \| R_{B2}) \| \beta R_E}.$$

Under the component assumptions in Equation (3.4), this transfer function is well-approximated by

$$\frac{R_{B1} \| R_{B2}}{\frac{1}{sC_I} + (R_{B1} \| R_{B2})}, \qquad \text{which is} \qquad \frac{s}{s + \frac{1}{(R_{B1} \| R_{B2}) C_I}}.$$

So, for half-power frequency f_L,

$$\frac{1}{2\pi\,(R_{B1} \| R_{B2})\, f_L} \leq C_I \leq 1\,\mu\text{F}. \tag{3.7}$$

To keep C_I small[7], let

$$20\,\text{Hz} \leq f_L \leq 35\,\text{Hz} \qquad \text{and} \qquad 10\,\text{k}\Omega \leq (R_{B1} \| R_{B2}) \leq 50\,\text{k}\Omega. \tag{3.8}$$

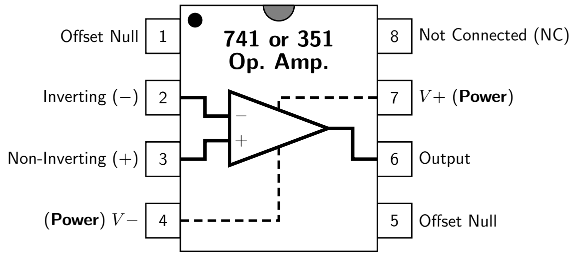
After tuning your circuit's gain and offset, be sure your half-power frequency is *no higher* than 35 Hz and increase C_I if needed.

Polarized capacitors: In our lab, large capacitors are only available as polarized electrolytic capacitors. If possible, keep C_I small so that you do not need a polarized capacitor. **Remember that large capacitors can be built with small capacitors wired in parallel.** If you absolutely *need* an electrolytic capacitor, **make sure you wire it correctly**. The capacitor must be wired so that its cathode (i.e., the "negative" end of the capacitor, shown in Figure 3.2 as a *curved* capacitor line) sees a lower DC potential than its anode[8] (the "positive" straight line). Because our input has negligible DC component and our base output has a ~1.483 V DC component, our input coupling capacitor should be wired with its cathode (i.e., "negative" end) toward the input.

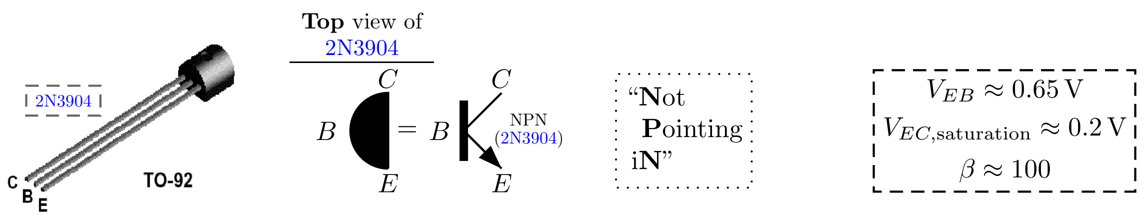
[7] $R_I = 1\,\text{k}\Omega$, $(R_{B1} \| R_{B2}) \approx 12.75\,\text{k}\Omega$ (i.e., $R_{B1} \approx 85\,\text{k}\Omega$ and $R_{B2} \approx 15\,\text{k}\Omega$), $C_I = 680\,\text{nF}$ (or $C_I = 470\,\text{nF}$), and $R_E = 10\,\text{k}\Omega$ are good starting choices.

[8] Remember that **A**node **C**urrent **E**nters (ACE), **C**athode **C**urrent **D**eparts (CCD), and **C**athodes are **C**urved.

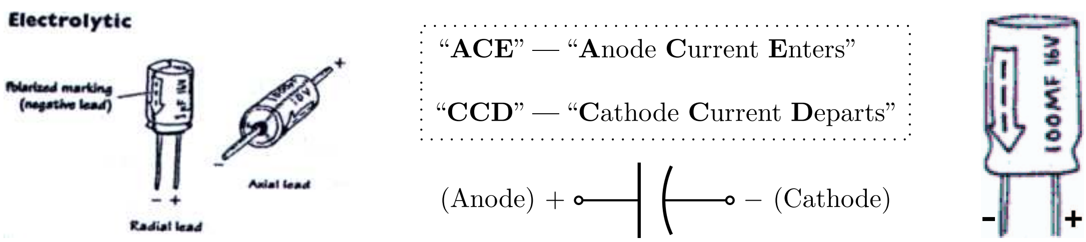
A Parts



(a) LM741/LF351 operational amplifier



(b) 2N3904 NPN BJT transistor



(c) Electrolytic capacitor

Figure A.1: Part pin-outs.