Current Sources and Ramp Generators

Lab 5: Analog-to-Digital Conversion

ECE 327: *Electronic Devices and Circuits Laboratory I*

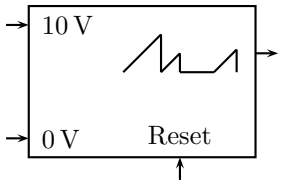
Abstract

For the analog-to-digital conversion lab, we need a resetable ramp generator. Here, we explore building a ramp generator from a current source. We implement a current source using an operational amplifier (Op Amp or OA) and then using a PNP transistor; the single-ended PNP source is used in the lab.

Contents

1 Introduction

Our goal is to build a circuit that maintains constant current i through a load L. In particular, we wish to use this component in a ramp generator like



The signals available to us are 10 V, 0 V, and a reset signal. The output should be a ramp train that resets to 0 V when the reset signal is asserted. The slope of the ramp is $(1/3)\,\mathrm{V}/\mu s$, and we assume the reset signal will be asserted when the ramp reaches 8 V or sooner.

Sawtooth generation: This ramp generator can be used to produce a sawtooth wave as well. Connect the ramp generator's reset input to a pulse that is asserted for a short instant at a regular period. As long as the time between pulses is not so long that the ramp generator saturates at its positive rail, the output will be a sawtooth.

2 Current Sources

Recall that a capacitor with capacitance C, current i_C, and potential difference v_C has transfer characteristics

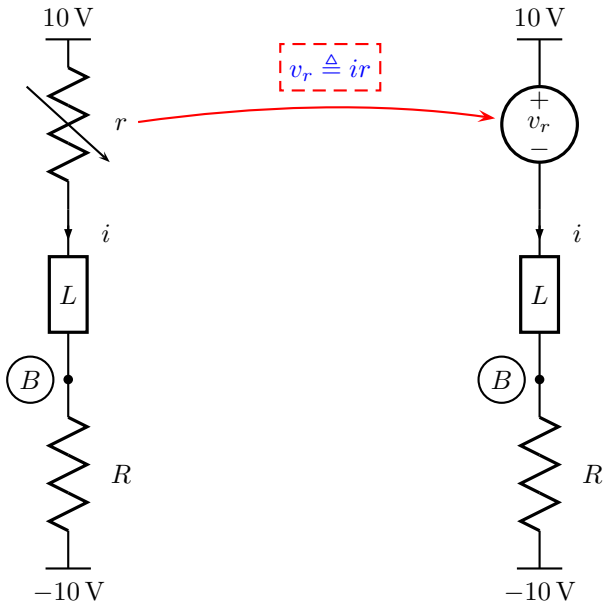
$$i_C = C\frac{\mathrm{d}\,v_C}{\mathrm{d}\,t}.$$

So an easy way to generate a potential ramp is to drive a constant current into a capacitor. Therefore, an important part of our ramp generator will be the current source.

We approach the problem of building a current source in two different but similar ways. The first method is implemented with an operational amplifier (Op Amp or OA) in section 3; the second method, which has better performance and does not require a -10 V rail, is implemented with a PNP transistor in section 4.

The Bottom Regulator

Consider the circuit in Figure 2.1(a) with resistor R, variable resistor r, and "bottom" node B shown. The



(a) Variable resistor model (b) Potential source model

Figure 2.1: Abstract "Bottom Regulating" Current Source: Circuit in (a) maintains current i through load L by continually adjusting variable resistor r to keep the potential at node B constant. Circuit in (b) is identical to circuit in (a), except the resistor r is replaced with a potential source v_r that serves the same purpose.

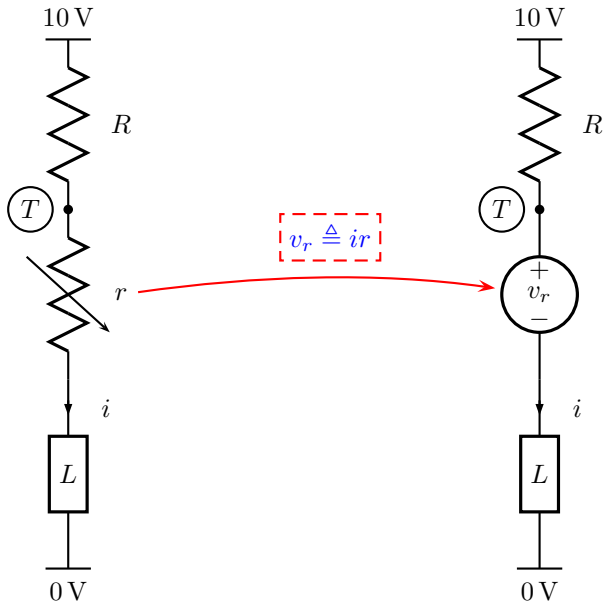
desired device will continually adjust the variable resistor r to maintain a constant potential v_B at node B. The equivalent device shown in Figure 2.1(b) adjusts the *positive* potential v_r to keep the potential at B constant. As long as L is sufficiently "small," the current i will be equal to $(v_B + (10\,\text{V}))/R$. That is, so long as the potential drop across load L is not too large, the current will be independent of the load and may be set by picking R. Unfortunately, there can be many practical problems with this implementation in real life. Additionally, **this method usually requires a negative rail**, which is not available to us.

The Top Regulator

Consider the more practical and better performing circuit in Figure 2.2(a) that rearranges resistor R, variable resistor r, and replaces "bottom" node B with "top" node T. The desired device continually adjusts variable resistor r to maintain constant potential v_T at node T. The equivalent device shown in Figure 2.2(b) adjusts the *positive* potential v_r to keep the potential at T constant. As long as L is sufficiently "small," current i will be equal to $((10\,\text{V}) - v_T)/R$. That is, so long as the potential drop across load L is not too large, the current will be independent of the load and may be set by picking R.

Current Source Compliance

If the load L is a 30 V battery, the potential source v_r needs to take a negative value. However, the potential source is implemented with a passive resistor, and so it cannot be negative. Similarly, if the load L is an infinite resistor (i.e., an open circuit), the current source will also fail because no potential v_r will be sufficient. The *compliance* of a current source is the output potential range over which the source is well-behaved. Circuits must be designed so that their current sources are always in compliance.



(a) Variable resistor model (b) Potential source model

Figure 2.2: Abstract "Top Regulating" Current Source: Circuit in (a) maintains current i through load L by continually adjusting variable resistor r to keep the potential at node T constant. Circuit in (b) is identical to circuit in (a), except the resistor r is replaced with a potential source v_r that serves the same purpose.

3 Operational Amplifier Bottom Regulation

Compare Figure 3.1 to Figure 2.1. The circuits are identical, but an operational amplifier has been used as the feedback device regulating the current. This circuit can perform poorly in practice or be completely

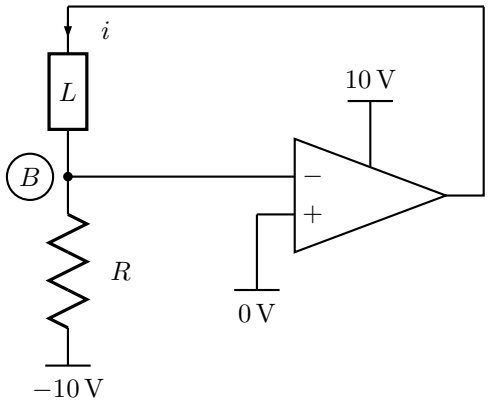


Figure 3.1: Operational Amplifier Current Source. The OA places a virtual ground at node B by driving a current i of $(10\,\mathrm{V})/R$ through the load L.

inappropriate. Because it requires a negative rail, it is inappropriate for our application; however, it is a good introductory example. The OA monitors the potential at node B and adjusts the resistance between 10 V and the load to keep current i constant at $(10\,\mathrm{V})/R$. To understand the concept of *compliance*, consider how the OA rails affect its ability to perform as a current source in this circuit. The low rail on this OA has not been drawn; however, it needs to be connected to properly bias the OA for operation (and compliance).

Ramp Generator

If a −10 V was available to us, the circuit in Figure 3.1 could be used to implement our ramp generator[1]:

- Replace the load L with a switch in parallel with a capacitor C.
- Close the switch whenever the reset signal is asserted.
- Use the output of the OA as the ramp signal.

The result is shown in Figure 3.2.

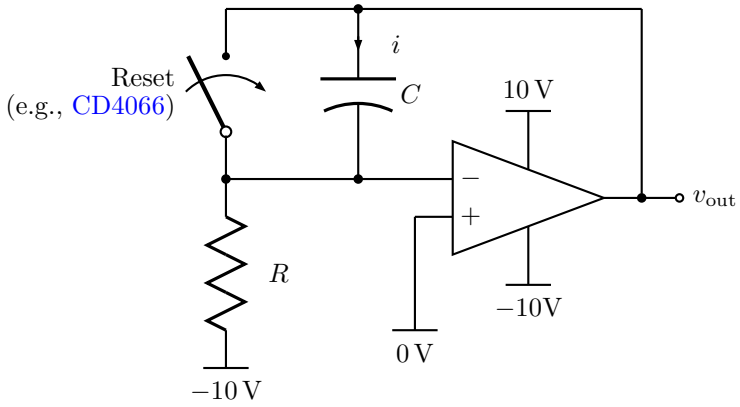


Figure 3.2: Operational Amplifier Ramp Generator. When switch is open, v_{out} rises linearly up to near 10 V. When switch is closed (i.e., reset is asserted), v_{out} is reset to 0 V. With a rail-to-rail OA, device compliance is approximately 0–10 V.

When the device is in *compliance*, the circuit output matches the potential across the capacitor, so

$$\frac{10\,\text{V}}{R} = i \qquad \text{and} \qquad i = Cv'_{out}. \tag{3.1}$$

Therefore, given capacitance C and desired slope v'_{out}, the current i (i.e., the resistance R) can be chosen. Of course, if the reset signal is not asserted before v_{out} reaches 10 V, the output will cease to be a ramp.

Ramp generator as integrator: When the reset switch is open, this operational amplifier circuit is an inverting integrator with a constant negative input. So it makes sense that the output has a constant positive slope. **To prevent offset-related problems**, before building your circuit, connect 10 kΩ potentiometer legs to OA "balance" pins and wiper to negative rail. Tune until shorted OA inputs produce no OA output.

Slew rate and input leakage: Real operational amplifiers are limited by their *slew rate*, the maximum rate of change of the operational amplifier's output. So the slew rate should be higher than the $(1/3)\,\text{V}/\mu s$ ramp slope, and the vertical edge trailing each output ramp will only be as steep as the slew rate. Also, any current leakage into the OA can affect the ramp slope and may lead to output offsets or drifting.

OA choice: The LM741 OA has a slew rate of $(1/2)\,\text{V}/\mu s$, so the trailing edge of each ramp will be too shallow (i.e., output may be triangular and/or have a nonzero minimum). The BiFET LF351, which has a $13\,\text{V}/\mu s$ slew rate and low gate leakage, may be a better choice in many applications. The BiMOS CA3160[2] has a $10\,\text{V}/\mu s$ slew rate and extremely low gate leakage, so it should be considered as well.

Switch choice: The CD4066 has four switches that each have nominal 80 Ω "on resistance." Remember that this on resistance affects the rate of the capacitor's discharge.

[1] Warning: In practice, this circuit is a poor ramp generator.
[2] If the CA3160 is not available, use a CA3130 with 56 pF across pins 1 and 8 (for lag compensation).

4 Transistor Top Regulation

A more efficient and often more practical way to generate a current is to use a properly-biased transistor. Recall that an NPN transistor can be used as a current sink and a PNP[3] transistor can be used as a current source. Because our ramp must be reset to a constant 0 V, we will need to use the "top regulating" current source shown in Figure 2.2, and so we will use a PNP current source.

Compare Figure 4.1 to Figure 2.2. The circuits are identical, but now a PNP transistor is the device

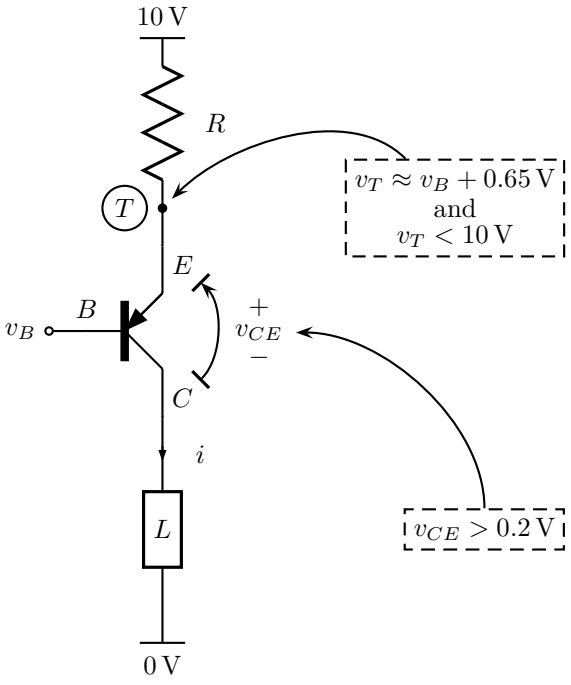


Figure 4.1: Generic PNP current source.

measuring the v_T potential at node T and adjusting the current through resistor R to maintain v_T at $v_B + 0.65\,\text{V}$. Note that because current is being "pushed" through the load rather than being "pulled" as in the operational amplifier example, the $-10\,\text{V}$ rail is not needed, so this circuit is ideal for our application.

Compliance and biasing: Because $v_{CE} > 0.2$ for the transistor to be in active mode, the compliance of this current source is from 0 V to roughly $v_B + 0.45\,\text{V}$. If the potential across the load L increases to above this value, the current i will cease to be constant. So the biasing potential v_B must be chosen high enough to ensure that the source stays in compliance while also keeping $v_T < 10\,\text{V}$. Therefore, the biasing potential v_B must be such that

$$v_{\text{comp}} - 0.45\,\text{V} < v_B < 9.35\,\text{V}$$

where v_{comp} is the upper limit of the compliance range. Note that the current into the *base* of the transistor is approximately 0 A (i.e., the base has very high impedance), which simplifies setting v_B.

[3] "**N**ot **P**ointing i**N**" (NPN) and "**P**oints i**N** **P**roudly" (PNP).

Resistor-Biased Ramp Generator

As discussed in section 3, the current source can be turned into our ramp generator by replacing the load L with a capacitor and switch in parallel. All that's left is setting the biasing potential v_B. In Figure 4.2, we do this with a resistive divider.

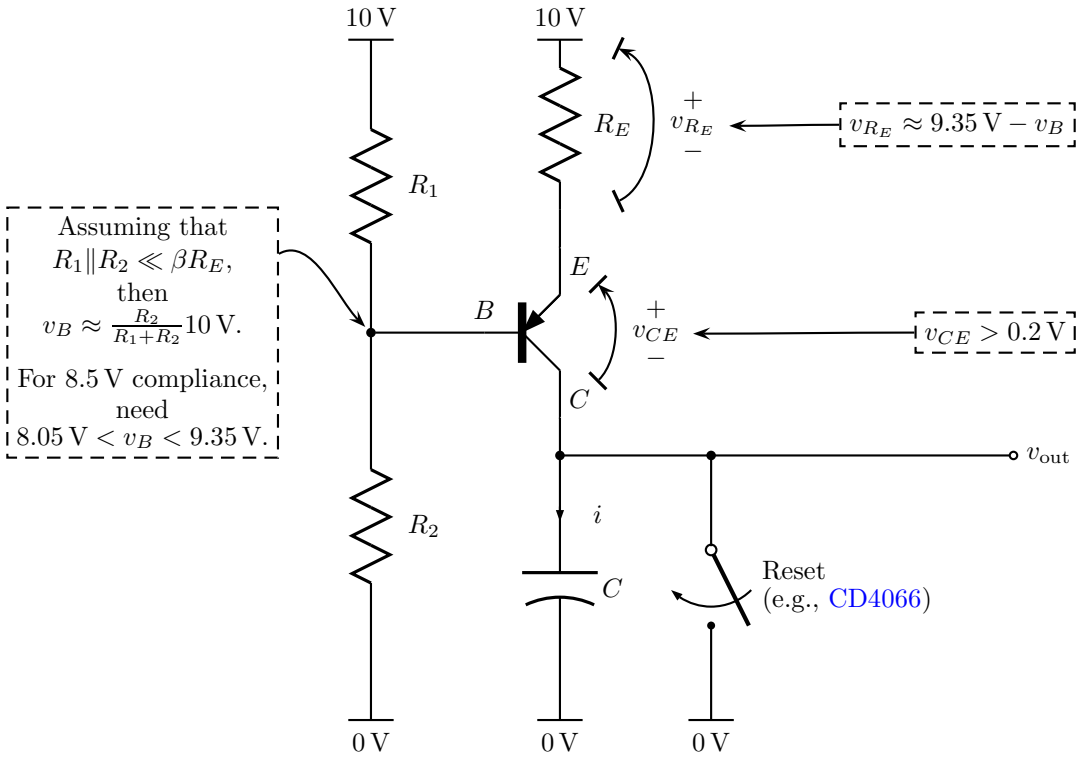


Figure 4.2: Resistive-divider-biased PNP BJT (e.g., 2N3906) ramp generator (0–8.5 V compliance).

For 8.5 V compliance, the biasing potential v_B must be so that $8.05\,\text{V} < v_B < 9.35\,\text{V}$. If R_1 and R_2 are picked so that

$$R_1 \| R_2 \ll \beta R_E \qquad \text{where} \qquad R_1 \| R_2 \triangleq \frac{R_1 R_2}{R_1 + R_2} \qquad \text{and} \qquad \beta \approx 100, \tag{4.1}$$

then

$$v_B \approx \frac{R_1}{R_1 + R_2} 10\,\text{V}.$$

The current through the load is set with *emitter* resistor R_E, where

$$\frac{9.35\,\text{V} - v_B}{R_E} = i \qquad \text{and} \qquad i = C v'_{\text{out}}.$$

Therefore, given capacitance C and desired ramp slope v'_{out}, the current i (i.e., the resistance R_E) can be chosen. This analysis depends on Equation (4.1) holding. Once the circuit is built and powered on, the reset signal must be asserted before v_{out} reaches 8.5 V or the transistor will saturate and the output will cease to be a ramp.

Implementation and Tuning: The circuit output should be tunable so that the actual slope observed in the laboratory can be adjusted. Implement the R_1–R_2 divider with a single potentiometer (i.e., where the middle "wiper" pin connects to the base of the transistor) so that the output current can be tuned. Alternatively, R_E can be implemented as a variable resistor (e.g., using two adjacent pins of a potentiometer).

Diode-Biased Ramp Generator

Another popular way of biasing PNP transistors in current sources is to set the base voltage multiple diode drops away from the positive rail. This method works well when diodes and transistors can be matched (e.g., when designing integrated circuits). Consider the configuration in Figure 4.3.

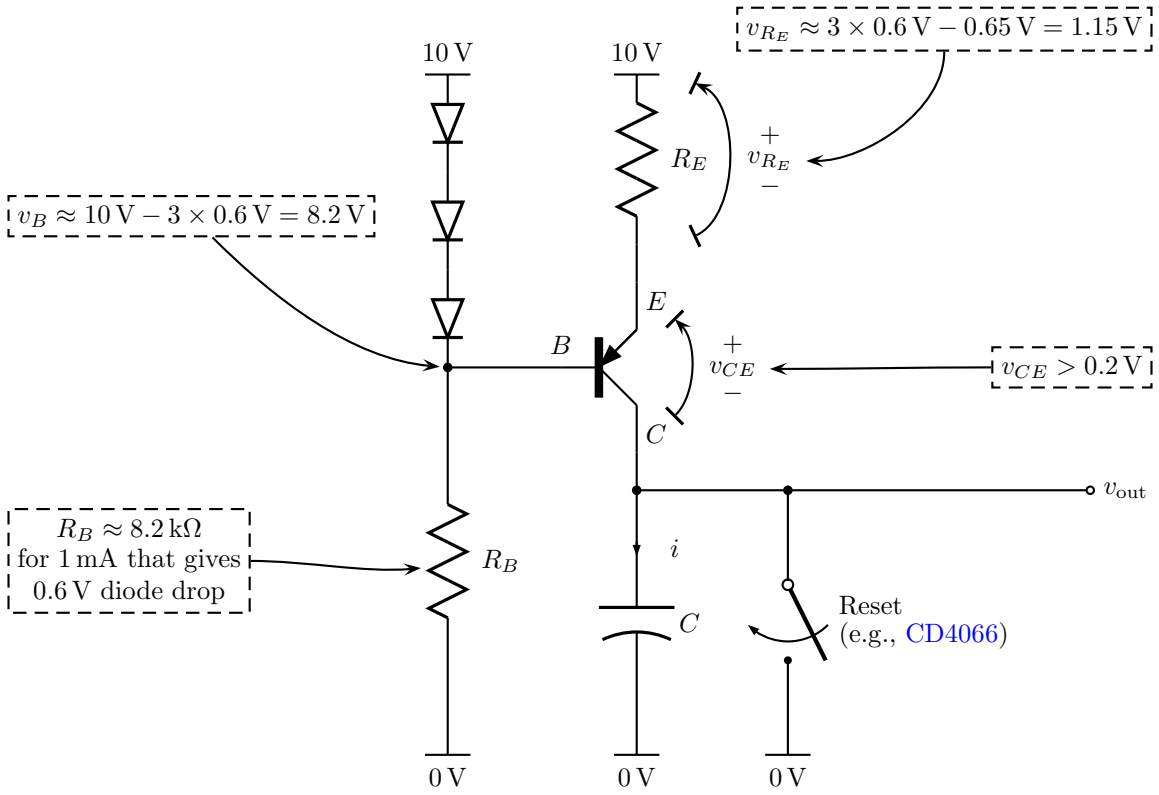


Figure 4.3: Diode-biased PNP BJT (e.g., 2N3906) ramp generator (0–8.65 V compliance).

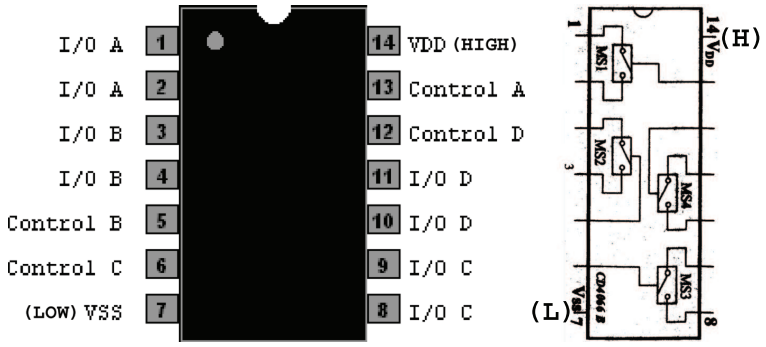
The suggested R_B value ensures that the current through the diodes is 1 mA, which is the typical forward current for the general purpose silicon diodes used in the laboratory. At this forward current, the potential drop across each diode is close to the nominal 0.6 V drop. Again, the current through the load is set with *emitter* resistor R_E, where

$$\frac{1.15\,\mathrm{V}}{R_E} = i \qquad \text{and} \qquad i = Cv'_{\mathrm{out}}$$

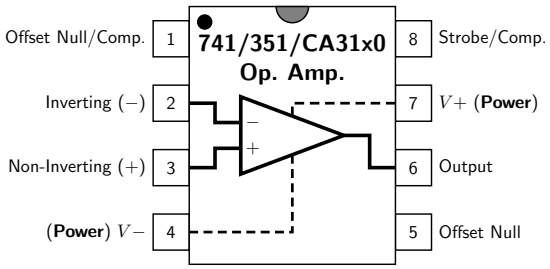
where $1.15\,\mathrm{V} = 10\,\mathrm{V} - 8.2\,\mathrm{V} + 0.65\,\mathrm{V}$. If these diodes were matched to the transistor, then the drop across the resistor would be two diode drops exactly. We can come close to this case (i.e., $v_R \approx 2 \times 0.65\,\mathrm{V}$) in the lab by using diode-connected transistors (i.e., transistors with collector and base shorted, a limiting case of the "Rubber diode" from the pre-quiz) instead of diodes.

Implementation and Tuning: The circuit output should be tunable so that the actual slope observed in the laboratory can be adjusted. Implement the emitter resistor R_E as a variable resistor (e.g., using two adjacent pins of a potentiometer) to tune the current. The biasing resistor R_B could also be tuned this way, but it will have less impact on the output than the R_E resistor.

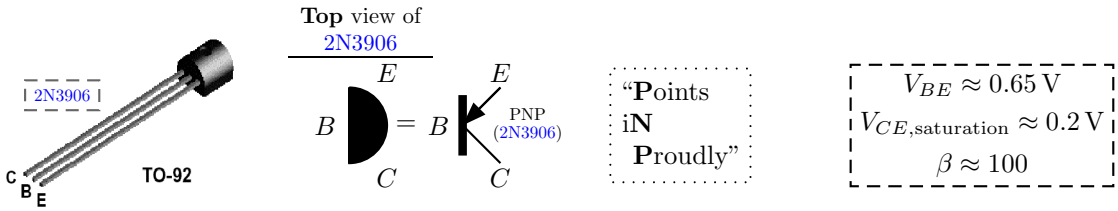
A Parts



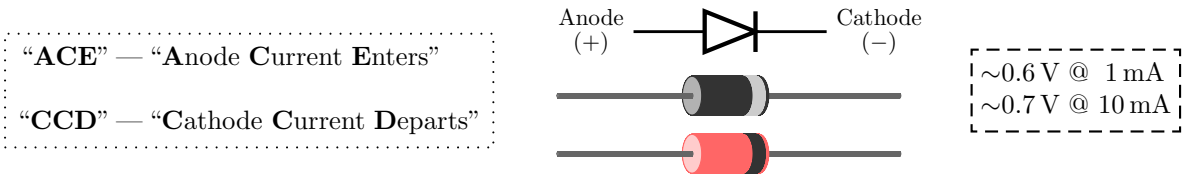
(a) CD4066 solid-state switch



(b) LM741/LF351/CA3160 operational amplifier



(c) 2N3906 PNP BJT transistor



(d) 1N914 silicon diode (generic small-signal diode)

Figure A.1: Part pin-outs.