Transistor-Based Ramp Generator

Lab 5: Analog-to-Digital Conversion

ECE 327: *Electronic Devices and Circuits Laboratory I*

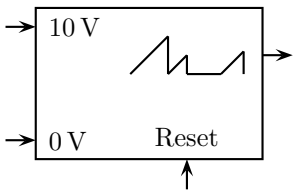
Abstract

For the analog-to-digital conversion lab, we need a resetable ramp generator. Here, we explore building a ramp generator from a current source. We show two implementations that both use a PNP current source.

Contents

1 Introduction

Our goal is to build a ramp generator like



The signals available to us are 10 V, 0 V, and a reset signal. The output should be a ramp train that resets to 0 V when the reset signal is asserted, and we assume that the reset signal will be asserted when the ramp reaches 8 V or sooner (i.e., the ramp generator has an 8 V *compliance*). We implement the ramp generator with a *pnp* current source that drives a capacitor that can be discharged with a switch.

Sawtooth generation: This ramp generator can be used to produce a sawtooth wave by connecting the ramp generator's reset input to a short pulse that is asserted at regular intervals. As long as the ramp generator does not saturate (i.e., go out of compliance) between pulses, the output will be a sawtooth.

PWM and Ramp Slope: The ramp generator will be used with a comparator to generate a pulse-width-modulated (PWM) signal.

(i) The ramp and PWM signal reset low on a ∼30 kHz clock with period $T \approx 33\,\mu$s.

(ii) The PWM signal transitions high whenever the ramp crosses the 2–8 V input from below.

(iii) The PWM signal drives a light-emitting diode (LED) that transmits to a detector equipped with a *Schmitt trigger* which gives it *hysteresis*. So PWM transitions must be **spaced at least** $6\,\mu$s **apart** to be detected (i.e., $6\,\mu$s is the minimum *negative pulse width* and *positive pulse width*).

So, after a reset, the ramp *must not* cross 2 V before $6\,\mu$s, and the ramp *must* cross 8 V *no later than* $(T - 6\,\mu\text{s}) \approx 27\,\mu$s. Hence, **the ramp slope** r **must be so that**

$$\boxed{0.297\,\frac{\text{V}}{\mu\text{s}} \approx \frac{8\,\text{V}}{27\,\mu\text{s}} \approx \frac{8\,\text{V}}{T - 6\,\mu\text{s}}} \leq r \leq \boxed{\frac{2\,\text{V}}{6\,\mu\text{s}} \approx 0.33\,\frac{\text{V}}{\mu\text{s}}}. \tag{1.1}$$

In practice, the actual "ramp" will be an exponential (due to capacitor and switch leakages) and the actual "ramp" slope may need to be slightly increased.

2 Transistor Top Regulation

Because the ramp must be reset to 0 V, we will hold one end of the load at 0 V and source current "from above" using a PNP current source[1]. We consider two different implementations of the topology in Figure 2.1.

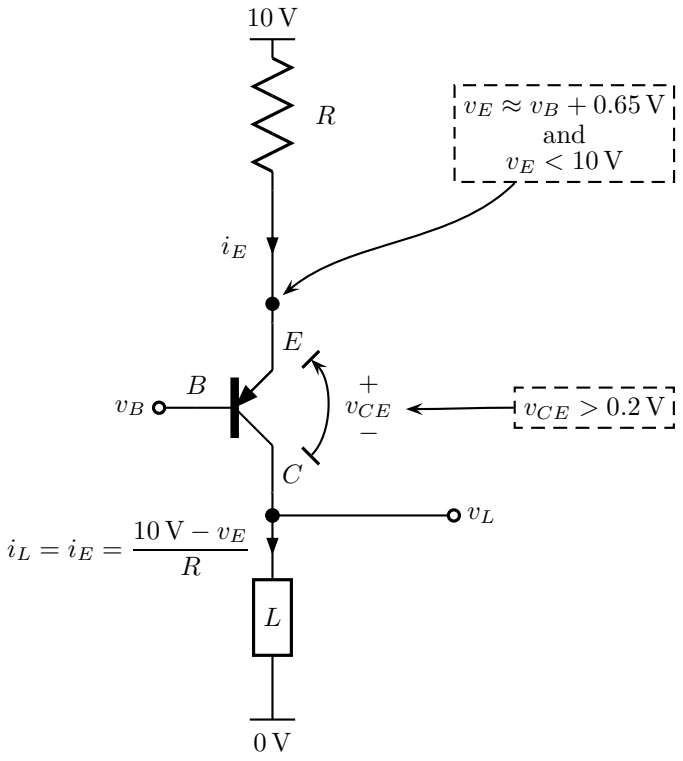


Figure 2.1: Generic PNP current source with load L and $v_B + 0.45\,\text{V}$ compliance.

Biasing: We need to choose a *biasing circuit* that sets v_B. The biasing circuit must have low impedance so that the small transistor base current makes little contribution to the value of v_B. The transistor will dynamically adjust its collector-to-emitter resistance so that the emitter potential v_E is $v_B + 0.65\,\text{V}$. In other words, it regulates the *current* i_L to be $(10\,\text{V} - (v_B + 0.65\,\text{V}))/R$.

Compliance: The transistor can only be in active mode if $v_{CE} > 0.2\,\text{V}$, and so this current source has a $v_B + 0.65\,\text{V} - 0.2\,\text{V}$ compliance. If the potential v_L rises above this value, the current i_L will fall below the desired value. So, given that $v_E < 10\,\text{V}$, v_B must be chosen high enough to ensure that the current source stays in compliance. Therefore, the biasing potential v_B must be such that

$$v_{\text{comp}} - 0.45\,\text{V} < v_B < 9.35\,\text{V}$$

where v_{comp} is the minimum required compliance (i.e., 8 V or 8.5 V for safety).

Ramp Generator: By replacing load L with a capacitor and switch in parallel, the circuit in Figure 2.1 with output v_L implements the ramp generator. The constant current causes the potential difference across the capacitor (i.e., v_L) to ramp, and the switch can discharge the capacitor before the output goes out of compliance. In the following, we implement this ramp generator using two different biasing circuits.

[1] Remember that transistor symbols "**P**oint i**N** **P**roudly" (PNP) or are "**N**ot **P**ointing i**N**" (NPN).

Resistor-Biased Ramp Generator

The ramp generator's current source can be biased with a low impedance resistive divider, as in Figure 2.2.

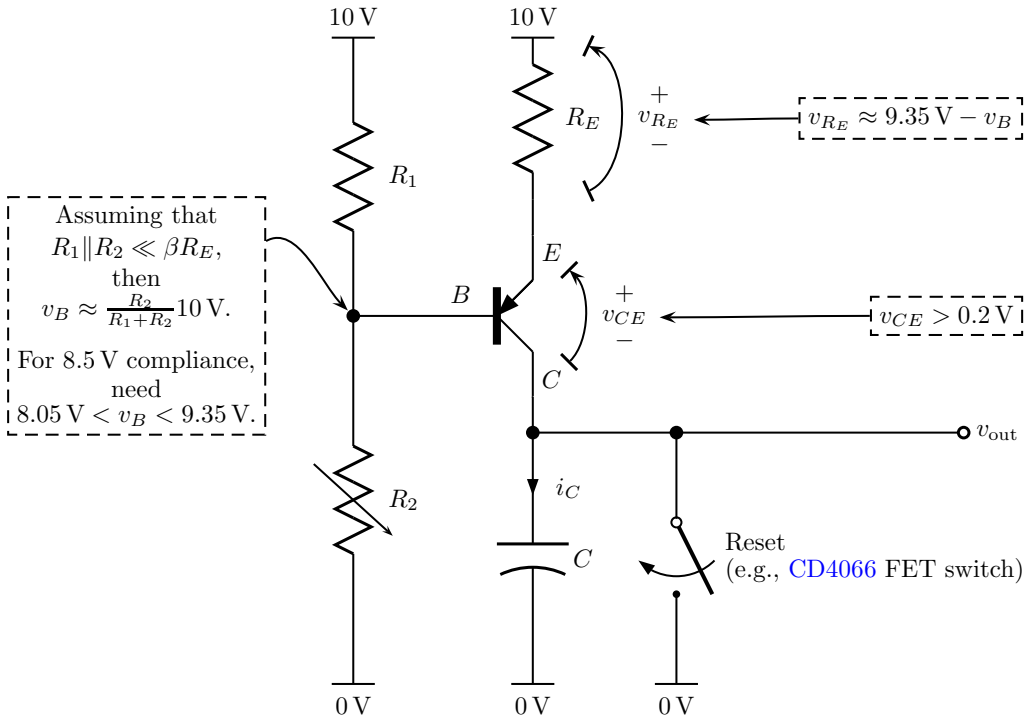


Figure 2.2: Divider-biased PNP (e.g., 2N3906) ramp generator (0–8.5 V compliance).

For 8.5 V compliance, the biasing potential v_B must be so that $8.05\,\text{V} < v_B < 9.35\,\text{V}$. To keep the biasing potential v_B independent of transistor base current, R_1 and R_2 should be chosen so that

$$R_1 \| R_2 \ll \beta R_E \qquad \text{where} \qquad R_1 \| R_2 \triangleq \frac{R_1 R_2}{R_1 + R_2} \qquad \text{and} \qquad \beta \approx 100, \tag{2.1}$$

and then the biasing potential

$$v_B \approx \frac{R_2}{R_1 + R_2} (10\,\text{V}) .$$

The current through the load is set with *emitter* resistor R_E, and so when the reset switch is *open*,

$$\frac{9.35\,\text{V} - v_B}{R_E} = i_C \qquad \text{and} \qquad i_C = C v'_{\text{out}}.$$

Therefore, given capacitance C (e.g., 2.2 nF) and a ramp slope v'_{out} as in Equation (1.1), the current i_C (i.e., the resistance R_E) can be chosen. This analysis depends on Equation (2.1) holding. Once the circuit is built and powered on, the reset signal *must* be asserted before v_{out} reaches 8.5 V or the transistor will saturate and the output will cease to be a ramp.

Implementation and Tuning: The circuit output should be tunable so that the actual slope observed in the laboratory can be adjusted. **Implement the R_1–R_2 divider with a single potentiometer** (i.e., where the middle "wiper" pin connects to the base of the transistor) so that the output current can be tuned.

Round Ramps and Exponential Resets: Real capacitors and switches have resistances that turn lines into exponential curves. If your reset edge is vertical but your ramp is curved, reconfigure your circuit for a larger C. Similarly, for an exponential reset with a very linear ramp, use a smaller C.

Diode-Biased Ramp Generator

Another popular way of biasing PNP transistors in current sources is to set the base voltage multiple diode drops away from the positive supply rail. When diodes are forward biased, they act as low impedance voltage sources, and so they provide a stiff biasing potential to the transistor (i.e., it is insensitive to the small transistor base current). This method works best when diodes and transistors (i.e., the transistor's base-emitter diode) can be matched (e.g., when designing integrated circuits). Consider the configuration in Figure 2.3.

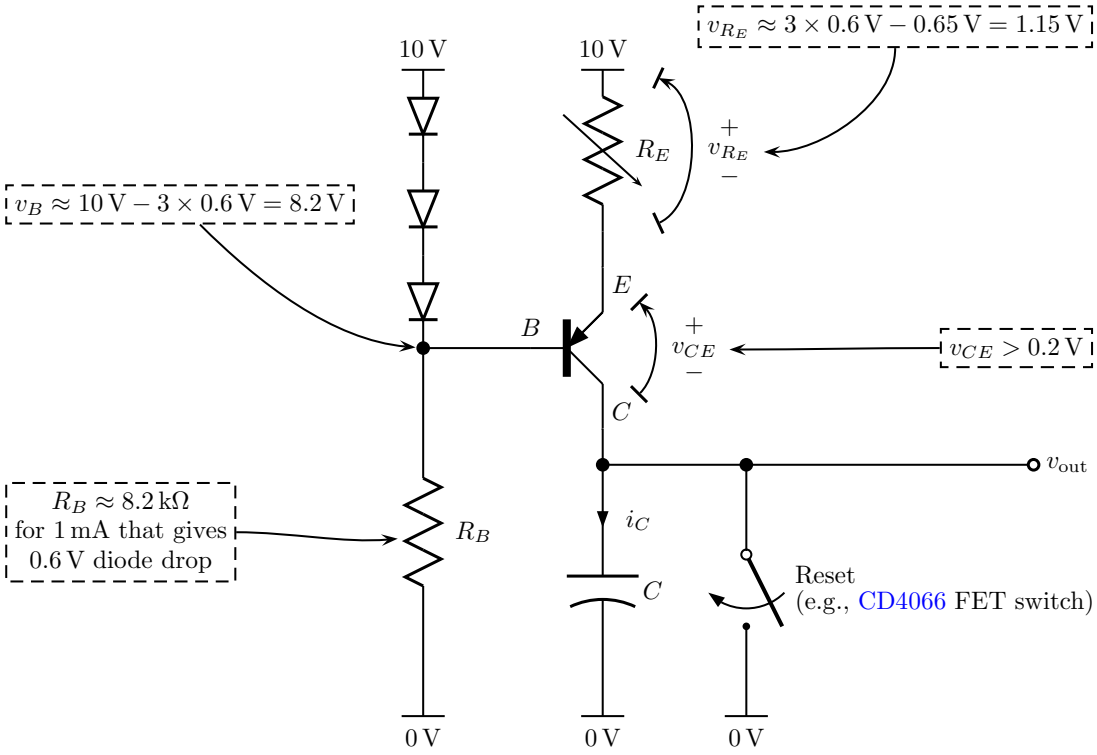


Figure 2.3: Diode-biased PNP (e.g., 2N3906) ramp generator (0–8.65 V compliance).

The suggested R_B value ensures that the current through the diodes is 1 mA, which is the typical forward current for the general purpose silicon diodes used in the laboratory. At this forward current, the potential drop across each diode is close to the nominal 0.6 V drop. **Decrease R_B if you observe low diode drops.** Again, the current through the load is set with *emitter* resistor R_E, and so when the switch is *open*,

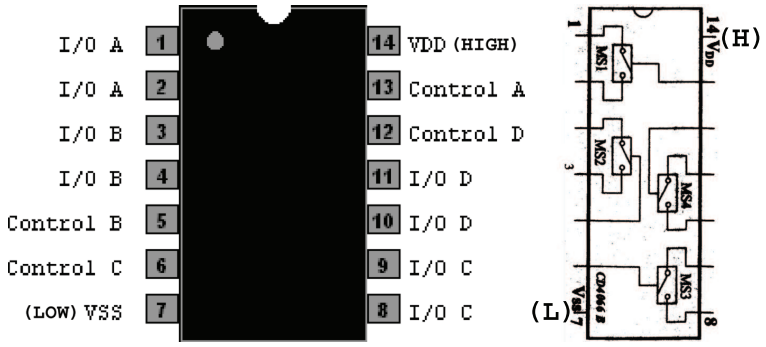
$$\frac{1.15\,\text{V}}{R_E} = i \qquad \text{and} \qquad i = Cv'_{\text{out}}$$

where $1.15\,\text{V} = 10\,\text{V} - 8.2\,\text{V} + 0.65\,\text{V}$. Therefore, given capacitance C (e.g., 2.2 nF) and ramp slope v'_{out} as in Equation (1.1), the current i (i.e., the resistor R_E) can be chosen.

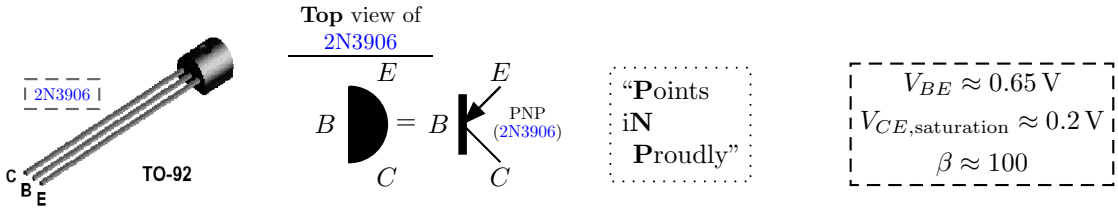
Implementation and Tuning: The circuit output should be tunable so that the actual slope observed in the laboratory can be adjusted. **Implement the emitter resistor R_E as a variable resistor** (e.g., using two adjacent pins of a potentiometer) to tune the current.

Round Ramps and Exponential Resets: Real capacitors and switches have resistances that turn lines into exponential curves. If your reset edge is vertical but your ramp is curved, reconfigure your circuit for a larger C. Similarly, for an exponential reset with a very linear ramp, use a smaller C.

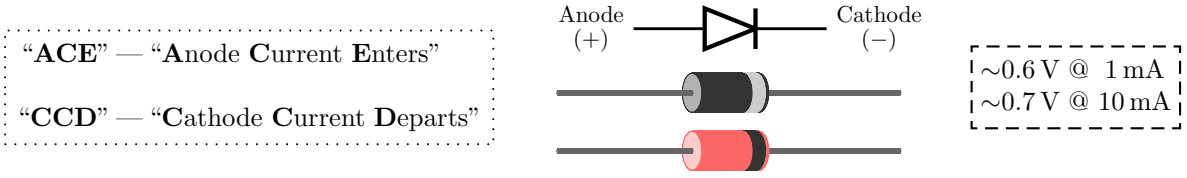
A Parts



(a) CD4066 solid-state switch



(b) 2N3906 PNP BJT transistor



(c) 1N914 silicon diode (generic small-signal diode)

Figure A.1: Part pin-outs.