Procedures and Explanations

Lab 3: Voltage Regulators

ECE 327: *Electronic Devices and Circuits Laboratory I*

Contents

Tear-off Pages: It may be helpful to tear off schematic, procedure, and data collection pages.

Report Strategies: **Make sure** to answer all questions brought up in the lab text's procedures. **Be sure** to compare regulation characteristics and comment on why they are similar or different. **Consider** presenting data from every regulator *together* (e.g., in one table/figure) to show similarities and differences.

1 Zener Diode Shunt Voltage Regulator

When an *ideal* diode is reverse biased, it conducts no current. The depletion layer at the reverse biased *pn* junction acts like an insulator[1]. Like any real insulator, it can suffer *breakdown* when the applied potential is sufficiently high.

A Zener[2] diode has been specially built so that its depletion layer breaks down (safely) at low voltages. At breakdown, the diode presents very little incremental resistance to current flow, and so it can act like a good voltage reference. Here, we build a simple Zener reference circuit.

Simple Zener Regulator Circuit

The circuit in Figure 1.1 maintains $\sim V_Z$ on its output by ***reverse*** biasing the Zener diode with $\sim I_Z$ current.

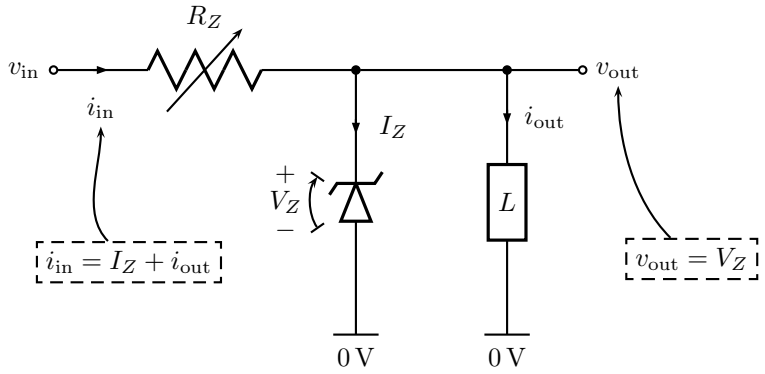


Figure 1.1: Zener diode shunt (i.e., parallel with load) voltage regulator with load L.

Typical V_Z, I_Z, and *"on" resistance* R_{on} for three Zener diodes in our laboratory are given in Table 1.1.

Zener:	$-V_Z$	R_{on}	@	$-I_Z$	($P_{Z,\text{max}}$ maximum)	($V_Z - I_Z R_{\text{on}}$)
1N4731:	−4.3 V	9 Ω	@	−58 mA	(1 Watt maximum)	(3.778 V)
1N5229:	−4.3 V	22 Ω	@	−20 mA	(0.5 Watt maximum)	(3.86 V)
1N751:	−5.1 V	17 Ω	@	−20 mA	(0.5 Watt maximum)	(4.76 V)

Table 1.1: Typical specifications for laboratory Zener diodes.

The resistor R_Z both biases the Zener diode and limits the output current i_{out}. That is,

$$v_{\text{out}} = v_{\text{in}} - (I_Z + i_{\text{out}})\, R_Z = v_{\text{in}} - \left(I_Z + \frac{V_Z}{L}\right) R_Z, \tag{1.1}$$

and so, for $v_{\text{out}} = V_Z$, R_Z must be chosen so that

$$R_Z = \frac{v_{\text{in}} - V_Z}{I_Z + i_{\text{out}}} = \frac{v_{\text{in}} - V_Z}{I_Z + \frac{v_{\text{out}}}{L}} = \frac{v_{\text{in}} - V_Z}{I_Z + \frac{V_Z}{L}}, \tag{1.2}$$

where L is the typical load (e.g., $\sim$10 kΩ) and v_{out} is the desired output. As the load L moves off of the typical load, the current through the Zener diode will change. A very small L will rob the Zener of so much current that it will move out of its Zener operation range. At that point, the output v_{out} will drop far below V_Z as the circuit reduces to a R_Z–L voltage divider.

[1] In fact, diodes share many similarities with capacitors. A *varactor*, also known as a *voltage controlled capacitor* or *variable capacitor* or simply a *varicap*, is nothing more than a diode specially made to exploit these similarities. Reverse biasing a varactor gives the designer a capacitance that is inversely proportional to the square root of applied reverse voltage.

[2] Physicist Clarence Zener (1905–1993) discovered the quantum mechanical tunneling effect responsible for the action in most Zener diodes. Bell Labs named the effect after him.

Zener Regulator Laboratory Procedure (figures and equations on page 2)

1. Design (i.e., choose components for desired output) and build the regulator in Figure 1.1 from page 2.
   - Lookup your Zener diode's I_Z and V_Z in Table 1.1.
     - Using a 4.3 V Zener diode will simplify later calculations.
     - **Make sure** you have the right Zener diode.
       * Diode part numbers (e.g., 1N5229) are written in **very small text** that is **"word-wrapped"** around the outside of the **glass diode package**. Rotate diode to read the text.
   - Use input $v_{\text{in}} = 15\,\text{V}$.
   - Use output $v_{\text{out}} = V_Z$.
   - Using Equation (1.2), calculate the R_Z needed to properly bias your Zener diode.
     - Use I_Z from Table 1.1.
     - Assume a typical load of $10\,\text{k}\Omega$.
2. **Verify proper regulator output**, but **DO NOT TUNE** the regulator.
   - Use a $10\,\text{k}\Omega$ load.
   - Use your digital multimeter (DMM) to measure the output.
     - If output is **far** from expected V_Z, make sure you calculated biasing resistor R_Z correctly.
   - **For your report**, refer to Equation (1.1) and discuss **how R_Z should be changed to tune the output (e.g., increase it or decrease it)**.
3. With no load (i.e., $L = \infty\,\Omega$, an *open* circuit), **record the i_{in} current measured by the power supply as the *no-load quiescent current***, which is the additional current required to operate the regulator with no load.
   - You can record this value below in the ∞ row of Table D.1 from Appendix D.
   - Few of the DC supplies display current precisely enough to make a good measurement of i_{in}, so **estimate** as best you can.
   - **DO NOT** use your DMM to make this measurement.
     - Few DMM ammeters in the lab are functional because their fuses are blown.
     - Using the DMM to measure current forces you to use the oscilloscope to measure DC output, which can be nontrivial.
4. Complete the tasks from Appendix C to measure the *load regulation* characteristics of the regulator.
   - You may use Table D.1 from page 19 to record your load regulation data.
   - Determine *load regulation*.
   - Determine *quiescent current (QC)* (i.e., operating current) *for each load*.
5. Complete the tasks from Appendix B to measure the *line regulation* characteristics of the regulator.
   - **IMPORTANT**: ***Disconnect*** DC supply from input and set load to $10\,\text{k}\Omega$.
   - Determine *dropout (DO) voltage*.
   - Determine *line regulation* in **both** units of V/V **and** %/V.
     - A regulator may have superior line regulation in V/V but not in %/V. Why?
   - Approximate *power-supply-ripple-rejection (PSRR) ratio*.
6. You will use the same Zener diode in Section 4. Otherwise, **you may** disassemble this circuit.
7. Continue by completing the procedures in Section 4 on page 8.

2 Discrete Pass-Transistor Series Voltage Regulator

DO NOT BUILD THIS CIRCUIT. This section is included to help you understand the circuits in Sections 4 and 5, which you *will* build.

The shunt voltage regulator described in Section 1 has poor load regulation. The resistor R_Z that biases the Zener diode also sources all of the load current, and so changes in the load modulate the Zener bias. Here, we use a transistor to isolate biasing resistor R_Z from the load. While improving the load regulation, the resulting *series* regulator (as opposed to the previous *shunt* regulator) has no ability to safely limit output current.

Series Voltage Regulator

The circuit in Figure 2.1 maintains a roughly constant v_{out} over a range of loads.

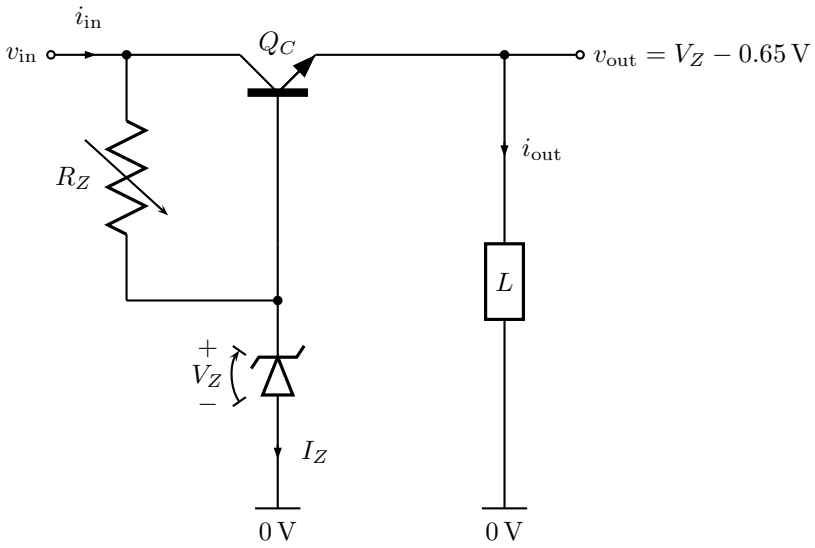


Figure 2.1: Discrete pass-transistor series voltage regulator with load L.

The *pass transistor* Q_C dynamically adjusts its collector–emitter resistance to keep the output one diode drop below the Zener voltage V_Z. In other words, Q_C **forms an** *npn* ***emitter follower*** **that** ***buffers*** **the Zener voltage**. If R_Z is chosen so that

$$R_Z = \frac{v_{\text{in}} - V_Z}{I_Z},$$

then

$$v_{\text{out}} = V_Z - 0.65\,\text{V} \tag{2.1}$$

where I_Z and V_Z are picked from Table 1.1. Unfortunately, the 0.65 V diode drop is strongly temperature dependent. As the output current i_{out} increases and power dissipation through Q_C increases, the 0.65 V in Equation (2.1) decreases. So

- load regulation is still imperfect,
- the circuit has no current-limiting ability, and
- the output of the circuit cannot be tuned.

In Sections 4 and 5, we address these issues by adding feedback to this circuit[3].

[3] An additional problem that we do not address is that the Q_C transistor has a low current gain (i.e., $\beta \approx 100$). To truly isolate the Zener diode, we need to use a very high gain transistor (with high current rating) or a Darlington/Sziklai configuration.

3 Discrete Transistor Adjustable Series Voltage Regulator

DO NOT BUILD THIS CIRCUIT. This section is included to help you understand the circuits in Sections 4 and 5, which you *will* build.

The voltage regulator in Section 2 improves upon the regulator in Section 1, but it still has imperfect load regulation and an output that cannot be tuned. In fact, because it has no feedback, it's arguably not a *regulator*. Here, we implement a feedback circuit around the simple pass-transistor reference circuit. Again, this circuit isolates the Zener from large changes in current draw, but the additional feedback will have gain that allows output to be tunable.

Adjustable Series Voltage Regulator with Feedback

The circuit in Figure 3.1 maintains a constant v_{out} over a range of loads. It is similar to the "*rubber Zener*" or "*rubber diode*" that we will use in the final laboratory in order to make our push–pull output stage a class-AB amplifier.

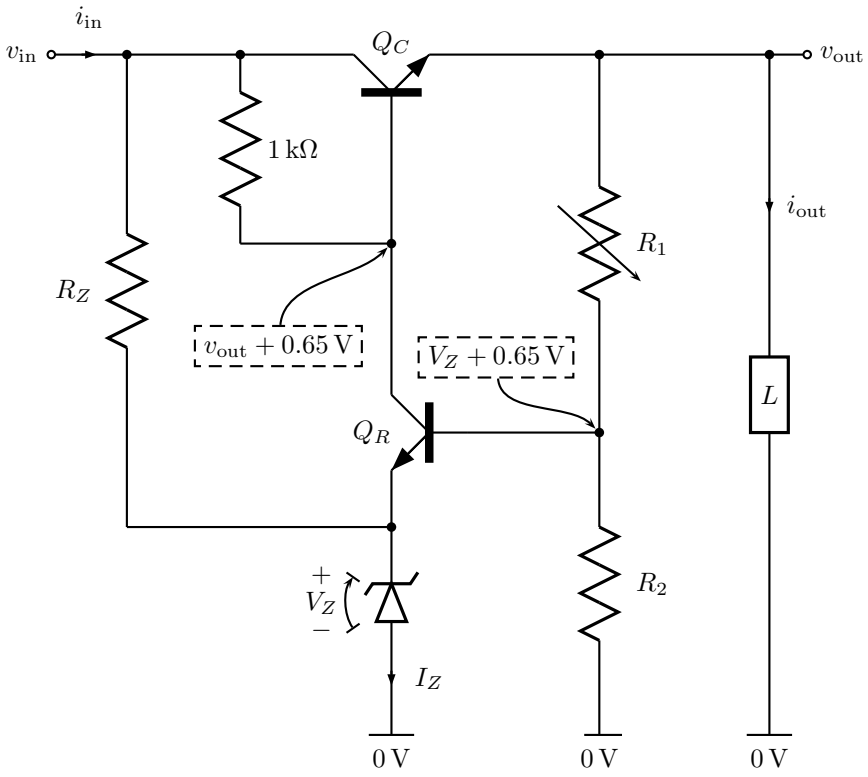


Figure 3.1: Discrete transistor adjustable series voltage regulator with load L.

This circuit builds on the simple pass-transistor approach from Section 2. Again, transistor Q_C sources *current* to the load. However, transistor Q_R is added to *regulate* the output. In particular, Q_R monitors v_{out} and adjusts the base of Q_C the correct amount of current is always being delivered to the R_1–R_2 divider to prop the output up at the desired value. Thus, the output is given by

$$v_{\text{out}} = \left(1 + \frac{R_1}{R_2}\right) \times (V_Z + 0.65\,\text{V}) \quad \text{so long as} \quad R_1 \| R_2 \ll \beta \times 1\,\text{k}\Omega \quad \text{and} \quad 1\,\text{k}\Omega \ll \beta\,((R_1 + R_2) \| L) \quad (3.1)$$

where V_Z and R_{on} come from Table 1.1 and L is a typical load (e.g., 10 kΩ). Changes in v_{in} show up as V_Z variations, and those variations are *amplified on the output*. So we might expect *line regulation* to *increase* from the simple Zener case. Regulation can be improved by connecting R_Z to v_{out} instead of v_{in}. Why?

Basic Analysis of Operation

The output v_{out} sends a current $v_{\text{out}}/(R_1 + R_2)$ through the R_1–R_2 divider, and the base of transistor Q_R monitors the center of that divider. Consider two cases to convince yourself that v_{out} has a unique stable equilibrium that we can set with R_1 and R_2 (which may be replaced with a potentiometer).

(i) When the center of the divider is greater than $V_Z + 0.65\,\text{V}$, Q_R pulls more current through the $1\,\text{k}\Omega$ resistor, which lowers the base of the Q_C resistor. As the Q_C base moves closer to its emitter (i.e., v_{out}), the current delivered through Q_C reduces, and less current is available for the R_1–R_2 divider. Thus, the drop across the R_2 resistor decreases and the Q_R base moves down toward $V_Z + 0.65\,\text{V}$.

(ii) When the center of the divider is less than $V_Z + 0.65\,\text{V}$, Q_R pulls less current through the $1\,\text{k}\Omega$ resistor, which raises the base of the Q_C resistor. As the Q_C base–emitter drop increases, the current delivered through Q_C increases, and more current is available for the R_1–R_2 divider. Thus, the drop across the R_2 resistor increases and the Q_R base moves up toward $V_Z + 0.65\,\text{V}$.

So when a heavy load (i.e., low resistance) robs R_1–R_2 of current, the regulator responds with more current.

Biasing for Operation

The resistor R_Z is chosen to provide the current I_Z to properly bias the Zener diode. However, because the Q_C-biasing $1\,\text{k}\Omega$ resistor also contributes Q_R collector current, the expression for I_Z is more complicated than in the previous regulators. In particular, the current I_Z is the sum of the current through the Q_R transistor and the R_Z resistor, which is

$$I_Z = \frac{v_{\text{in}} - (v_{\text{out}} + 0.65\,\text{V})}{1\,\text{k}\Omega} + \frac{v_{\text{in}} - V_Z}{R_Z}.$$

So, using values from Table 1.1, R_Z should be chosen so that

$$R_Z = \frac{v_{\text{in}} - V_Z}{I_Z - \frac{v_{\text{in}} - v_{\text{out}} - 0.65\,\text{V}}{1\,\text{k}\Omega}}. \tag{3.2}$$

As previously discussed, the R_1–R_2 divider resistors should be chosen so that

$$v_{\text{out}} = \left(1 + \frac{R_1}{R_2}\right) \times (V_Z + 0.65\,\text{V}) \quad \text{so long as} \quad R_1 \| R_2 \ll \beta \times 1\,\text{k}\Omega \quad \text{and} \quad 1\,\text{k}\Omega \ll \beta\,((R_1 + R_2) \| L) \tag{3.3}$$

where L is a typical load (e.g., $10\,\text{k}\Omega$). The two inequalities ensure that Q_R and Q_C biasing current is negligible, which makes the design simpler and more robust. In particular, the feedback "gain" will only be set by R_1 and R_2 and the Q_R transistor will have maximal control authority over Q_C. Note that decreasing $R_1 + R_2$ increases the power dissipation of the divider (i.e., the *quiescent current*).

Tradeoffs

To keep Q_C (and Q_R) active, its base must sit one base–emitter drop (e.g., $0.65\,\text{V}$) above the output, so expect a low *dropout voltage* of $\sim 0.65\,\text{V}$ or *less*[4]. Because v_{out} amplifies variations in V_Z caused by variations in v_{in}, the circuit has poorer *line regulation* (in V/V) than the Zener regulator[5]. However, v_{out} is immune to increases in *load*, so this circuit has very low *load regulation*. In fact, the circuit is unable to safely *limit* output current. In Sections 4 and 5, we sacrifice excellent load regulation in order to limit current.

Assuming Q_C base current is negligible, the input current i_{in} is given by

$$i_{\text{in}} = \underbrace{\frac{v_{\text{in}} - V_Z}{R_Z} + \frac{v_{\text{in}} - (v_{\text{out}} + 0.65\,\text{V})}{1\,\text{k}\Omega}}_{I_Z} + \underbrace{\frac{v_{\text{out}}}{R_1 + R_2}}_{\substack{\text{Divider} \\ \text{Current}}} + \underbrace{\frac{v_{\text{out}}}{L}}_{i_{\text{out}}}$$

which is similar to the expression for i_{in} for the simple Zener regulator, except that the R_1–R_2 divider always draws current from the output. So having a robust and adjustable output requires more power[6].

[4] Because Q_C is in "series" with the output, it dissipates a lot of heat. So its base–emitter drop may be closer to $0.5\,\text{V}$.
[5] Line regulation can be improved by connecting R_Z to the steady v_{out} — Zener current will not vary *as much* with v_{in}.
[6] Compare to the power–distortion tradeoff in amplifier design.

4 Current-Limited Discrete Transistor Series Voltage Regulator

The adjustable voltage regulator described in Section 3 is a major improvement over the simple Zener regulator in Section 1. By dissipating extra power, the regulator was able to robustly maintain a programmable output. Unfortunately, the discrete transistor adjustable regulator from Section 3 does not provide any protection for short-circuit events. Here, we add a single transistor and resistor that sense the output current and throttle it when reaches a programmable threshold. Of course, this modification degrades the *load regulation* of the circuit.

Adjustable Series Regulator with Current Limiting

The circuit in Figure 4.1 maintains a constant v_{out} over a range of loads that require sufficiently small current. Outside of that range, v_{out} is throttled to limit current.

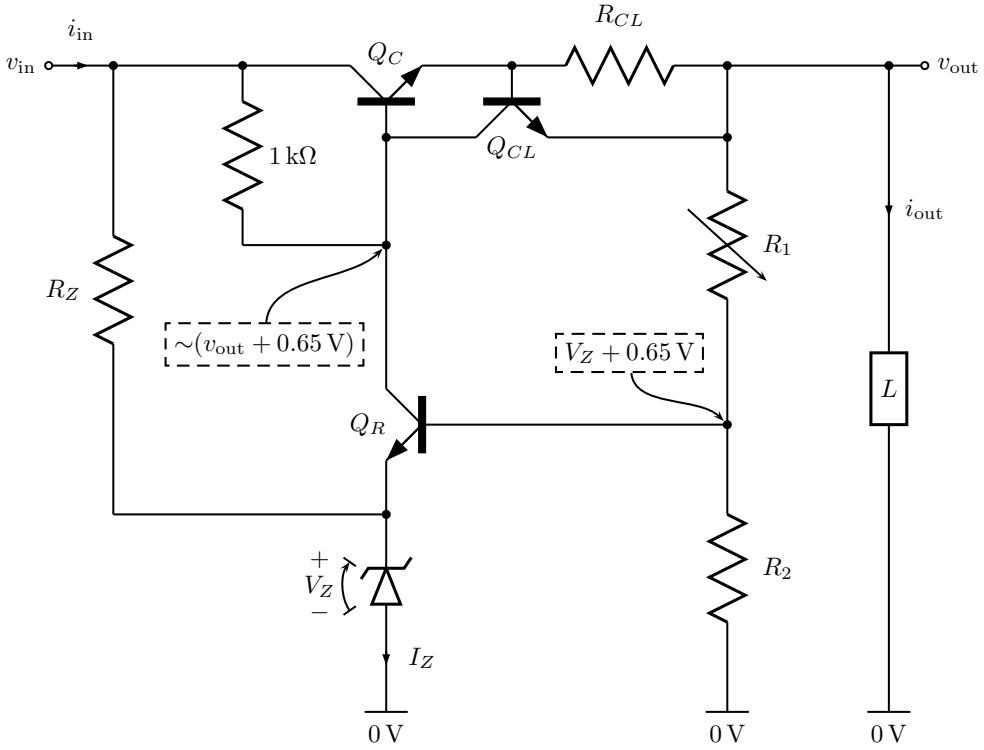


Figure 4.1: Discrete transistor current-limited adjustable series voltage regulator with load L.

The Q_{CL} transistor is normally cutoff, and so it usually can be ignored. So the values of R_Z, R_1, and R_2 are still determined by Equations (3.2) and (3.3)[7]. When the current i_{out} is great enough to put a $\sim$0.5 V drop across the the R_{CL} resistor, Q_{CL} *starts* to move out of cutoff and pulls more current through the 1 kΩ resistor. This Q_{CL} current lowers the Q_C base, which causes Q_C to reduce its collector–emitter current (i.e., its collector–emitter resistance increases and v_{out} falls so that the Q_C emitter *continues* to stay a diode drop away from the Q_C base). As v_{out} falls, Q_R goes into cutoff and Q_{CL} gains complete control over Q_C. In active mode, Q_{CL} won't allow its base–emitter drop to rise over 0.65 V, and so the output current will have a maximum limit[8] of

$$i_{\text{SC}} = \frac{0.65\,\text{V}}{R_{CL}}. \tag{4.1}$$

By choosing R_{CL}, the designer has control over the maximum short-circuit current for the output.

[7] These statements are not entirely true. The R_{CL} resistor actually reduces the biasing current to the Zener diode by a load-dependent amount. In other words, for short-circuit protection, we tradeoff good load regulation. Compare this tradeoff with the power–distortion tradeoff with amplifiers.

[8] Because resistance of metals increases with temperature, the measured limit may *appear* to be larger.

Limited Regulator Laboratory Procedure (figures and equations on page 7)

1. Design (i.e., choose components for desired output) and build the regulator in Figure 4.1 from page 7.
   - Use the Zener diode from Section 1.
   - Use input $v_{\text{in}} = 15\,\text{V}$ and output $v_{\text{out}} = 10\,\text{V}$.
   - Use Equation (3.2) to choose the new Zener biasing resistor R_Z.
   - Pick the R_1–R_2 divider resistors as in Equation (3.3).
     - The divider can be implemented as a **potentiometer** where the middle "wiper" pin connects to the base of the transistor.
     - A 2 kΩ (code: `202` or `2k`) or a 5 kΩ (code: `502` or `5k`) potentiometer is a **good choice**.
   - Use short-circuit current $i_{\text{SC}} = 30\,\text{mA}$ with Equation (4.1) to pick current-limiting resistor R_{CL}.
2. **Tune the regulator output** by adjusting R_1 and R_2 until measured $v_{\text{out}} \approx 10\,\text{V}$.
   - Use a 10 kΩ load.
   - Use your digital multimeter (DMM) to measure the output.
   - Refer to Equation (3.1).
     - Use R_1–R_2 divider to change the gain on $(V_Z + 0.65\,\text{V})$.
     - Note that adjusting R_Z changes V_Z (should be ∼4.3 V or ∼5.1 V depending on diode).
3. With no load (i.e., $L = \infty\,\Omega$, an *open* circuit), **record the i_{in} current measured by the power supply as the *no-load quiescent current***, which is the additional current required to operate the regulator with no load.
   - You can record this value below in the ∞ row of Table D.2 from Appendix D.
   - Few of the DC supplies display current precisely enough to make a good measurement of i_{in}, so **estimate** as best you can.
   - **DO NOT** use your DMM to make this measurement.
     - Few DMM ammeters in the lab are functional because their fuses are blown.
     - Measuring DC output potential with the oscilloscope is nontrivial. Don't tie up the DMM.
4. Complete the tasks from Appendix C to measure the *load regulation* characteristics of the regulator.
   - You may use Table D.2 on page 20 to record your load regulation data.
   - Determine *load regulation* (low, but not perfect *by design* (for report: explain why)).
   - Determine *quiescent current (QC)* (i.e., operating current) *for each load*.
   - **MAKE SURE** that output current is limited near i_{SC} (limiting starts near $10\,\text{V}/L \approx 0.5\,\text{V}/R_{CL}$).
     - **DO NOT CONTINUE** unless your regulator limits current correctly.
     - If your regulator does not limit current, make sure your Q_{CL} transistor is *npn* type and does not have collector and emitter reversed.
   - Short-circuit current may **appear** to be larger than 30 mA; hot resistors take-on *higher* resistances.
5. Complete the tasks from Appendix B to measure the *line regulation* characteristics of the regulator.
   - Determine *dropout (DO) voltage* (should be 0.5–0.7 V (for report: why?)).
   - Determine *line regulation* in **both** units of V/V **and** %/V.
     - Line regulation in V/V should be **twice** Zener line regulation. Why?
     - Even though V/V worse than Zener, %/V is equal (or better). Why? Significance?
     - Think about why connecting R_Z to v_{out} instead of v_{in} will improve line regulation.
   - Approximate *power-supply-ripple-rejection (PSRR) ratio*.
6. **Most of this circuit** will be used in Section 5, and so **you should not disassemble** the circuit.
7. Continue by completing the procedures in Section 5 on page 10.

5 Discrete Transistor Series Voltage Regulator with Foldback

The adjustable voltage regulator described in Section 4 works well, but the maximum current occurs at the short-circuit condition, which forces the regulator to dissipate a great deal of heat. Here, we modify the current-limiting circuitry to implement *current foldback* so that the short-circuit current is less than the maximum current. This modification improves load regulation, allows more power to be safely delivered to the load, and protects the regulator from excessive heat dissipation on a short circuit.

Adjustable Series Regulator with Current Foldback

The circuit in Figure 5.1 maintains a constant v_{out} over a range of loads that require sufficiently small current. The Q_{FB} current-foldback transistor replaces the Q_{CL} current-limiting transistor from Section 4.

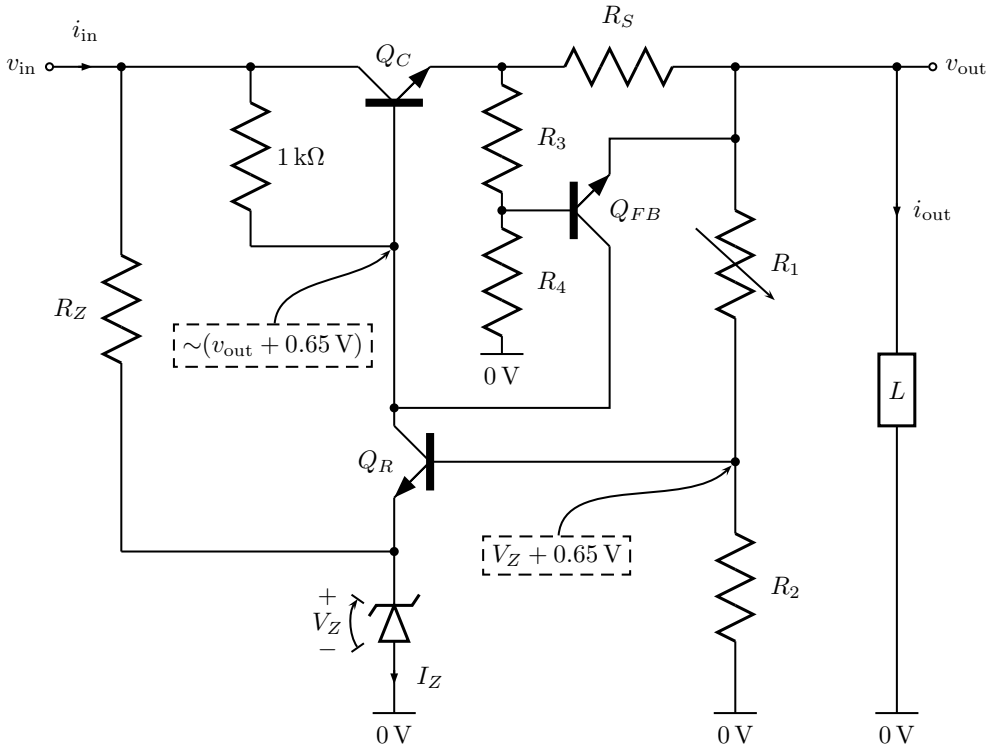


Figure 5.1: Discrete transistor current-foldback adjustable series voltage regulator with load L.

Notice that the Q_{FB} transistor and Q_{CL} transistors only differ in their base connection. Rather than sensing the R_S drop directly, the Q_{FB} transistor base is attached to a resistive divider, and so it becomes active at a different stage than the Q_{CL} transistor current limiter. Because the R_3–R_4 divider draws additional current, quiescent current will be higher than in the simple current limiter case.

The short-circuit output current i_{SC} and the maximum current i_{FB} are such that

$$R_S = \frac{v_{\text{out}}}{i_{\text{SC}}\left(1 + \frac{v_{\text{out}}}{0.65\,\text{V}}\right) - i_{\text{FB}}}. \tag{5.1}$$

The R_3–R_4 divider resistors should be chosen (a potentiometer can be used as well) so that

$$\frac{R_3}{R_4} = \frac{R_S \times i_{\text{SC}}}{0.65\,\text{V}} - 1 \quad \text{so long as} \quad R_3 \| R_4 \ll \beta \times 1\,\text{k}\Omega \quad \text{and} \quad 1\,\text{k}\Omega \ll \beta(R_3 + R_4). \tag{5.2}$$

By choosing R_S, R_3, and R_4, the designer can place the maximum current i_{FB} away from the short-circuit event. Power dissipated in the regulator is roughly constant for loads that would normally require $i_{\text{out}} \geq i_{\text{FB}}$.

Foldback Regulator Laboratory Procedure (figures and equations on page 9)

1. Design (i.e., choose components for desired output) and build the regulator in Figure 5.1 from page 9.
   - Start with the circuit in Figure 4.1 from Section 4.
     - Again, use input $v_{\text{in}} = 15\,\text{V}$ and output $v_{\text{out}} = 10\,\text{V}$.
     - Use the **same** R_Z from Equation (3.2) and the **same** R_1–R_2 divider resistors as in Equation (3.3).
   - **To convert** Q_{CL} **to** Q_{FB}, disconnect base of Q_{CL}, insert R_3–R_4 divider, and swap R_{CL} for R_S.
     - Use **foldback current** $i_{\text{FB}} = 150\,\text{mA}$ **and short-circuit current** $i_{\text{SC}} = 50\,\text{mA}$ with Equation (5.2) to pick resistors R_S, R_3, and R_4.
     - Do **NOT** use a potentiometer for R_3 and R_4. **They *cannot be tuned*** — their values should be *SET* **before** installing them (i.e., pick two discrete resistors close to desired values).
2. Tune the regulator output by adjusting R_1 and R_2 until measured $v_{\text{out}} \approx 10\,\text{V}$.
   - **IDEALLY**, very little *new* tuning should be required.
   - Use your digital multimeter (DMM) to measure the output for a $10\,\text{k}\Omega$ load.
   - Again, refer to Equation (3.1).
     - Use the R_1–R_2 divider to change the gain on $(V_Z + 0.65\,\text{V})$.
     - Note that adjusting R_Z changes V_Z (should be $\sim$4.3 V or $\sim$5.1 V depending on diode).
3. With no load (i.e., $L = \infty\,\Omega$, an *open* circuit), **record the** i_{in} **current measured by the power supply as the *no-load quiescent current*** (i.e., additional current required for unloaded operation).
   - You can record this value below in in the ∞ row of Table D.3 from Appendix D.
   - Few of the DC supplies display current precisely enough to make a good measurement of i_{in}, so **estimate** as best you can.
   - **DO NOT** use your DMM to make this measurement.
     - Few DMM ammeters in the lab are functional because their fuses are blown.
     - Doing so forces you to use the oscilloscope to measure DC output, which can be nontrivial.
4. Complete the tasks from Appendix C to measure the *load regulation* characteristics of the regulator.
   - You may use Table D.3 on page 21 to record your load regulation data.
   - Determine *load regulation*.
   - Determine *quiescent current (QC)* (i.e., operating current) *for each load*.
   - **DO NOT CONTINUE** unless **output** current i_{out} folds back near i_{FB} and is limited near i_{SC}.
     - Foldback may not occur **until very late** (e.g., smallest two resistors in table).
     - If your regulator never folds back:
       - Make sure Q_{FB} transistor is *npn* and does not have collector and emitter reversed.
       - Make sure R_3–R_4 divider doesn't have R_3 and R_4 swapped.
     - If your regulator folds back early:
       - Make sure R_S resistor is not too large (e.g., don't mistake colors for $1.5\,\text{k}\Omega$ and $15\,\Omega$).
       - Make sure R_3/R_4 ratio is not too small.
5. Complete the tasks from Appendix B to measure the *line regulation* characteristics of the regulator.
   - As long as load resistance is not very small (e.g., $L = 10\,\text{k}\Omega$), **RESULTS SHOULD BE *IDENTICAL* to simple current-limited case** (i.e., preceding case without foldback). Why?
   - Determine *dropout (DO) voltage*.
   - Determine *line regulation* in **both** units of V/V **and** %/V.
   - Approximate *power-supply-ripple-rejection (PSRR) ratio*.
6. None of this circuit will be used in the rest of the laboratory. **You may disassemble it completely.**
7. Continue by completing the procedures in Section 6 on page 12.

6 LM317 Adjustable Positive Series Voltage Regulator

For an electron to conduct across a diode, it must be equipped with enough energy to move from semiconductor's *valence band* to the *conduction band*. This "*bandgap*" is approximately 1.25 eV for silicon[9]. That is, 1.25 V (i.e., 1.25 J/C) must be placed across a silicon diode to sustain an electric current.

Electrons in our laboratory are pre-loaded with energy from the ambient temperature of the room, and so laboratory diodes require only 0.6–0.7 V for conduction. Less electrical tension is required to be pull them across the diode. A diode requires 1.25 V for conduction only at *absolute zero* (0 K or −273.15°C).

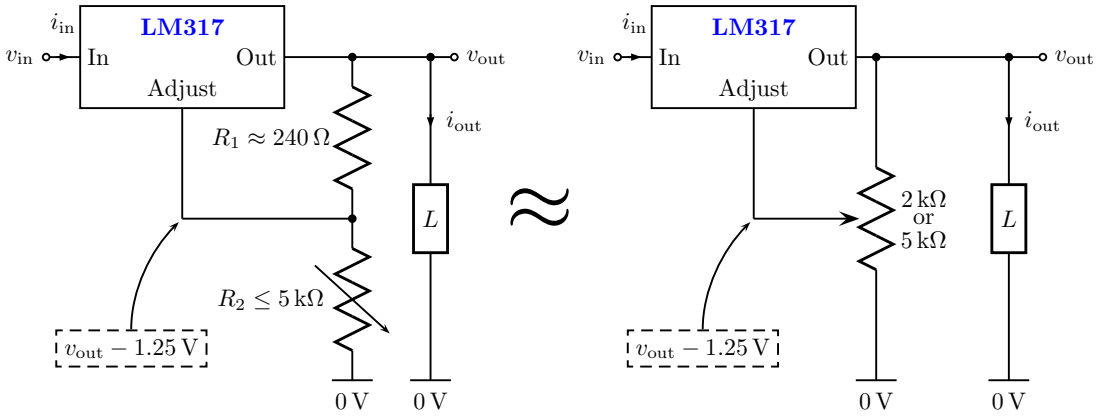
It should not be surprising that voltage references have *temperature dependence*. For example, references based on diode drops will give different outputs for different temperatures, as explained above. A *bandgap reference* compensates for this temperature dependence. Here, we describe the basic bandgap reference theory and then introduce the LM317 adjustable positive series voltage regulator. This off-the-shelf (OTS) circuit has negligible temperature dependence for most applications and a maximum current[10] of 1.5 A.

Bandgap Reference Theory

The V_{BE} of a transistor has a *negative temperature coefficient*—the energy required to conduct across the base–emitter diode of a transistor *decreases* as temperature *increases*. So even when the potential across a base–emitter diode is constant, if temperature increases, electrons require less energy for conduction, and so collector–emitter current *increases*. Therefore, the collector–emitter current has a *positive temperature coefficient*. Matched transistors can be combined so that current increases from the latter effect create increasing potentials that balance the decreasing V_{BE} from the former effect. The result is a 1.25 V (i.e., an *absolute zero* diode drop) reference that is nearly immune to temperature variation. A resistive divider can amplify that reference, which yields an adjustable temperature-independent voltage regulator.

Simple LM317 Series Regulator Circuit

The two circuits in Figure 6.1 are identical. The LM317 maintains 1.25 V potential difference between its "`Out`" and "`Adjust`" pins, and the voltage divider acts as a lever propping v_{out} above the ground reference.



(a) Using variable-resistor divider. (b) Using potentiometer.

Figure 6.1: LM317 adjustable series voltage regulator with load L. Use $40\,\text{V} > (v_{\text{in}} - v_{\text{out}}) > 3\,\text{V}$.

In Figure 6.1(a), the (temperature-independent) output is given by

$$v_{\text{out}} \quad = \quad (1.25\,\text{V}) \times \frac{R_1 + R_2}{R_1} \quad = \quad (1.25\,\text{V}) \times \left(1 + \frac{R_2}{R_1}\right). \tag{6.1}$$

The less conventional circuit in Figure 6.1(b) may also be used (with caution).

[9] A better approximation for the silicon bandgap is 1.22 eV.
[10] *External* current limiting or foldback can be added (e.g., to protect *downstream* components). LM317 datasheet has details.

LM317 IC Regulator Laboratory Procedure (figures and equations on page 11)

1. Design (i.e., choose components for desired output) and build the regulator in Figure 6.1(a) or 6.1(b) from page 11.
   - **RESISTOR VALUES SHOWN** in schematics reflect nominal *potentiometer* sizes.
   - **CONSTRUCT REGULATOR *COMPACTLY* NEAR *CORNER* OF BREADBOARD.**
   - Again, use input $v_{\text{in}} = 15\,\text{V}$ and output $v_{\text{out}} = 10\,\text{V}$.
   - Use Equation (6.1) to calculate the proper $R_1/(R_1 + R_2)$ ratio.
   - You have two implementation options.
     (i) From Figure 6.1(a), set $R_1 \approx 240\,\Omega$ and calculate R_2. Implement R_2 with a variable resistor made from adjacent legs of a $2\,\text{k}\Omega$ or $5\,\text{k}\Omega$ potentiometer.
     (ii) From Figure 6.1(b), adjust a $2\,\text{k}\Omega$ or $5\,\text{k}\Omega$ potentiometer for the right $R_1/(R_1 + R_2)$ ratio.

     While **you should perform all calculations for your report**, it may be easiest to **skip calculations *for now*** and tune $2\,\text{k}\Omega$ or $5\,\text{k}\Omega$ potentiometer until output reaches desired 10 V.
   - Potentiometer codes: $2\,\text{k}\Omega \triangleq$ `202` or `2k` and $5\,\text{k}\Omega \triangleq$ `502` or `5k`
2. Tune regulator output by adjusting the R_1–R_2 divider (or potentiometer) until measured $v_{\text{out}} \approx 10\,\text{V}$.
   - Use a $10\,\text{k}\Omega$ load.
   - Use your digital multimeter (DMM) to measure the output.
   - Refer to Equation (6.1).
3. Use your DMM to **measure (and RECORD) the potential between the `Output` and `Adjust` pins**. What is expected?
4. With no load (i.e., $L = \infty\,\Omega$, an *open* circuit), **record the i_{in} current measured by the power supply as the *no-load quiescent current***, which is the additional current required to operate the regulator with no load.
   - You can record this value below in the ∞ row of Table D.4 from Appendix D.
   - Few of the DC supplies display current precisely enough to make a good measurement of i_{in}, so **estimate** as best you can.
   - **DO NOT** use your DMM to make this measurement.
     – Few DMM ammeters in the lab are functional because their fuses are blown.
     – Using the DMM to measure current forces you to use the oscilloscope to measure DC output, which can be nontrivial.
5. Complete the tasks from Appendix C to measure the *load regulation* characteristics of the regulator.
   - You may use Table D.4 on page 22 to record your load regulation data.
   - Determine *load regulation* (should be very good).
   - Determine *quiescent current (QC)* (i.e., operating current) *for each load* (should be very low).
6. Complete the tasks from Appendix B to measure the *line regulation* characteristics of the regulator.
   - Determine *dropout (DO) voltage* (expect $\sim$1 V for this $10\,\text{k}\Omega$ load).
   - Determine *line regulation* in **both** units of V/V **and** %/V (should be nearly perfect).
   - Approximate *power-supply-ripple-rejection (PSRR) ratio*.
7. You will use this regulator (and one more like it) in Section 8 and in the rest of the quarter. **DO NOT** disassemble it.
8. Continue to Section 8 on page 15 **if there's time**.
   - If you are out of time, you will have to complete Section 8 at some time later in the quarter. There is no need to complete Section 8 for the lab report.

7 Improving Dynamic Performance

Real loads have both resistive and reactive components that can change rapidly over time. Also, between an ideal regulator and its load, a small amount of series inductance between the two can be detrimental to circuit performance. For example, consider a load that requires a sudden injection of current. Series inductance between load and regulator prevents the instant change in current and actually generates an electromotive force (i.e., a "voltage") countering the change. The result is that the potential seen by the load drops significantly. Furthermore, when the same problem exists between a regulator and *its* supply, a fast clock supplied by a regulator with a high dropout voltage or poor ripple rejection can couple clock signal energy into every analog output of the circuit. That is, the regulator will have poor *load transient response*.

Capacitively Bypassing Dynamic Signals

A perfect voltage reference signal is purely DC, and so we can short circuit its AC part to ground. In other words, after power-up transients die out, we do not suffer any performance losses by adding *bypass capacitors* to ground at every point in a circuit where the reference should be steady.

Capacitors provide low impedance to high frequencies. A pin delivering power to (or from) a component has some small series resistance, so placing a capacitor from that pin to ground forms a voltage divider that transfers very little AC power into (or out of) the part. That is, most of the AC power *bypasses* the pin and is returned directly to ground. The larger the capacitor, the lower the high frequency impedance.

Consider the time-domain case. At power-up, the capacitor stores a large quantity of "reserve charge" for when components need extra current that is not quickly available from the power supply. Because of the high capacitance, the capacitor can source a large current to the destination without much change in potential. Similarly, the capacitor can sink a large current without much change in potential. The capacitor "stiffens" the power rail by acting like a dynamic battery.

Practical Implementation

Large capacitors are expensive and require time and power to initially charge up. So there are a few rules of thumb about where and how they should be added. Additional rules exist about capacitor dielectric choice.

Large at Source: The largest power bypass capacitors should be placed at the output of your power supply (even if it's not regulated). Consider putting your ugliest and most expensive capacitors (e.g., aluminum electrolytic capacitors in our lab) here. Capacitances can be large (e.g., 1–300 μF). **Pay attention to capacitor polarity; wiring a polarized capacitor backwards across a DC supply can cause explosions or fires.** If you are bypassing a negative supply rail, remember that the ground should be connected to the capacitor's anode (i.e., "positive" end).

Small at Sink: Place smaller bypass capacitors (e.g., .1–2 μF) directly at component supply pins.

Capacitors in Parallel: To increase capacitance, *reduce series resistance*, and *reduce cost*, use multiple smaller capacitors in *parallel* rather than using one large capacitor. Stiff power supplies often have "banks" of bypass capacitors connected in parallel. Printed circuit boards sometimes have portions of capacitor banks left unpopulated to allow the designer to add or remove capacitors during prototyping without changing the schematic.

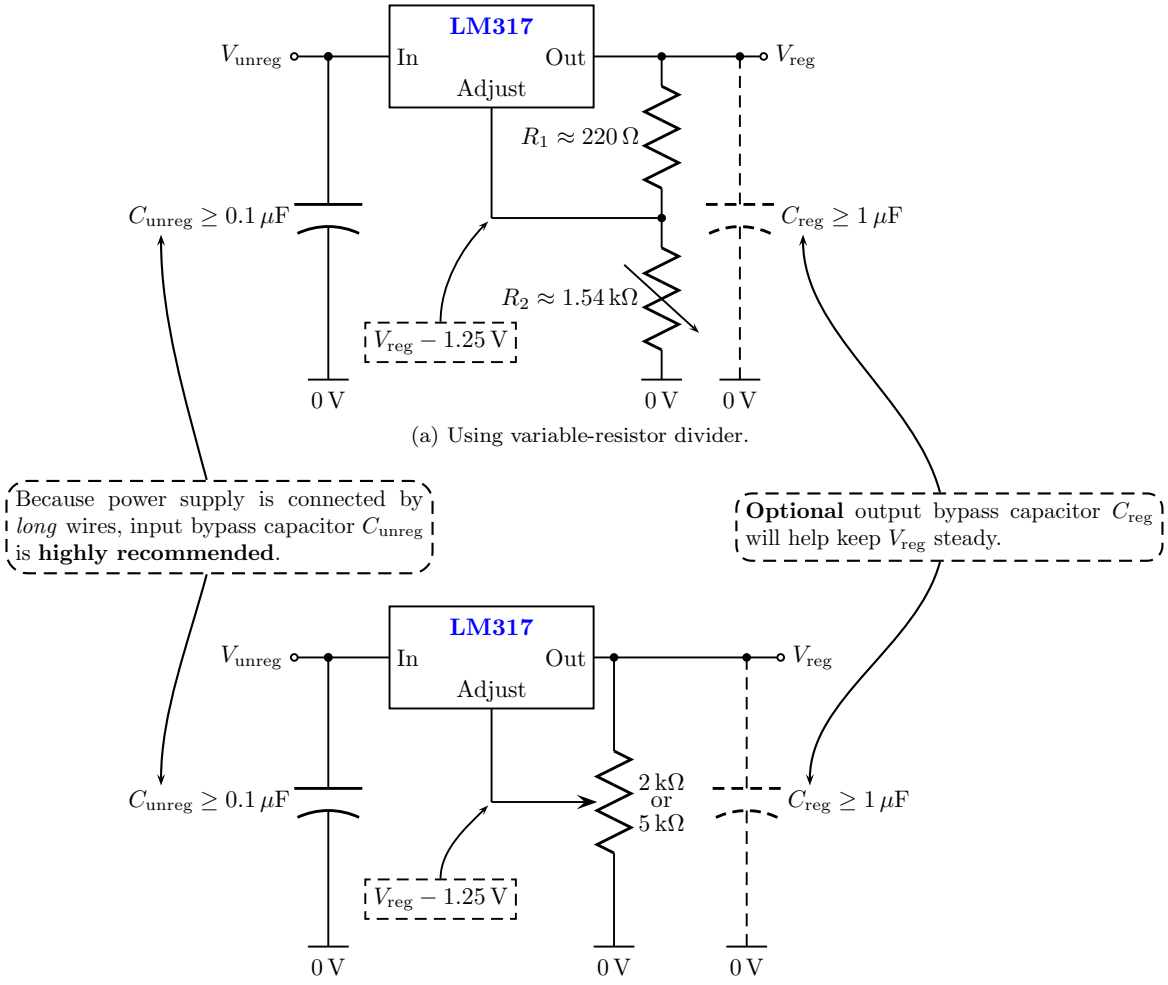
Divider Bypassing: When voltage dividers are used to tune regulator output, use a bypass capacitor across the resistor going to ground in order to stabilize the reference point.

Protection Diodes: To prevent capacitive discharging into the regulator, protection diodes (i.e., reverse-biased diodes placed strategically to give current an alternate discharge path when output is short circuited) may be used.

Good regulation is more important to some components than others. Regions of your circuit can be given stiffer power signals than others. Low noise designs have separate ground planes, specially routed return paths, and even separate power supplies.

8 Project Regulators

In the class project, we will use a version of the regulator introduced in Section 6 to implement two $10\,V_{DC}$ regulated supplies, one for our transmitter and one for our receiver. However, for reasons discussed in Section 7, we use a regulator shown in Figure 8.1, which has added *bypass capacitors*.



(a) Using variable-resistor divider.

(b) Using potentiometer.

Figure 8.1: LM317 adjustable voltage regulator. Use $V_{unreg} \approx 15\,V$ and set $V_{reg} \approx 10.0\,V$.

In Figure 8.1(a), the output

$$V_{reg} = (1.25\,V) \times \left(1 + \frac{R_2}{R_1}\right). \tag{8.1}$$

The circuit in Figure 8.1(b) may also be used with caution. In either circuit, input capacitor $C_{unreg} \approx 0.1\,\mu F$ should be used to steady the input supply rail. Output capacitor $C_{reg} \approx 1\,\mu F$ may be used if artifacts are being coupled into circuit signals via the supply (e.g., clock noise). Also, a $\sim 0.1\,\mu F$ capacitor to ground can be placed at the 10 V input to each circuit component. Finally, an additional **large** bypass capacitor (e.g., 1–10 μF) *near* LM317 from `Adjust` to ground can improve both *load transient* performance and PSRR.

Protection Diodes: Whenever bypass capacitors are used with a regulator, there is a risk that it will be damaged on a short circuit event when the capacitors discharge through it. So *protection diodes* that are *reverse biased* under normal operation can be added for protection by providing an alternate path for capacitor current. See LM317 datasheet for more information. Pay attention to `Adjust` capacitor protection.

Construction of Voltage Regulator for Project (Enhanced LM317)

If time permits, complete the following.

⋆ **YOU MAY USE** your LM317 regulator from Section 6 as a starting point for **ONE** of these TWO regulators. In that case, you'll just need to **add bypass capacitors** and make sure the output is **tuned** well.

1. Design, build, and tune a $10\,V_{DC}$ regulator from Figure 8.1 for the project's *transmitter*. Notice the *bypass capacitors*.
   - Assemble the regulator **compactly** in one of the **corners** of your breadboard (i.e., near the *transmitter* area of your breadboard).
   - **Tune** your regulator by adjusting its R_1–R_2 potentiometer until the output is between 9.99 V and 10.01 V.
   - You may load your regulator with $10\,k\Omega$ while tuning it, but you should remove the load when finished.
   - Make sure your **regulator input** is **easy to identify**. You will use it during **every lab** to power your circuit.
     - Consider connecting it to one of the *banana connectors* at the top of your breadboard.
     - The banana connectors can *plug* directly into the DC power supply.
   - You will **never** connect the DC power supply to the rails on your breadboard.
     - Connect your regulator **output** to your breadboard rails.
     - **Isolate** one set of rails for your *transmitter* components.
       - For convenience, you **may** connect transmitter and receiver **grounds**.
2. Design, build, and tune a $10\,V_{DC}$ regulator from Figure 8.1 for the project's *receiver*. Notice the *bypass capacitors*.
   - Assemble the regulator **compactly** in one of the **corners** of your breadboard (i.e., near the *receiver* area of your breadboard, far from the *transmitter* side).
   - **Tune** your regulator by adjusting its R_1–R_2 potentiometer until the output is between 9.99 V and 10.01 V.
   - You may load your regulator with $10\,k\Omega$ while tuning it, but you should remove the load when finished.
   - Make sure your **regulator input** is **easy to identify**. You will use it during **every lab** to power your circuit.
     - Consider connecting it to one of the *banana connectors* at the top of your breadboard.
     - The banana connectors can *plug* directly into the DC power supply.
   - You will **never** connect the DC power supply to the rails on your breadboard.
     - Connect your regulator **output** to your breadboard rails.
     - **Isolate** one set of rails for your *receiver* components.
       - For convenience, you **may** connect transmitter and receiver **grounds**.

It may be a good idea to locate these regulators **far apart** or **on separate breadboards** so that plenty of space remains for the rest of the circuit.

If you do not have time to complete these circuits, build them at your convenience before the end of the quarter. **You will be reminded to complete these circuits in each of the following labs.**

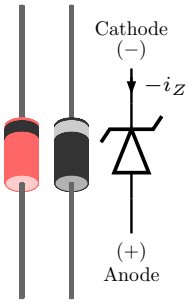
A Parts

For *conventional* ***forward*** current i_Z:

"**CCD**" — "**C**athode **C**urrent **D**eparts"

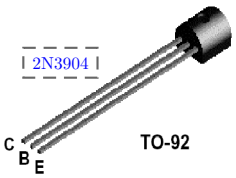
"**ACE**" — "**A**node **C**urrent **E**nters"

Reverse $(I_Z, V_Z) = (-i_Z, -v_Z)$.

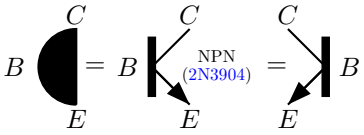


Zener:	$-V_Z$	R_{on}	@	$-I_Z$	($P_{Z,\max}$ maximum)	($V_Z - I_Z R_{\text{on}}$)
1N4731:	−4.3 V	9 Ω	@	−58 mA	(1 Watt maximum)	(3.778 V)
1N5229:	−4.3 V	22 Ω	@	−20 mA	(0.5 Watt maximum)	(3.86 V)
1N751:	−5.1 V	17 Ω	@	−20 mA	(0.5 Watt maximum)	(4.76 V)

(a) 1N4731/1N5229/1N751 Zener diode



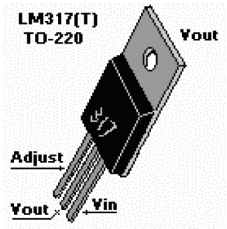
Top view of 2N3904

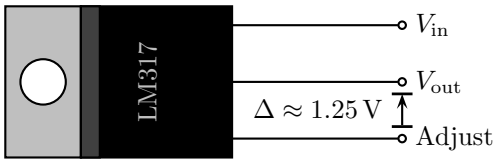


"**N**ot **P**ointing i**N**"

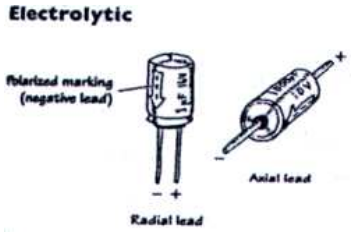
$V_{EB} \approx 0.65\,\text{V}$
$V_{EC,\text{saturation}} \approx 0.2\,\text{V}$
$\beta \approx 100$

(b) 2N3904 NPN BJT transistor





(c) LM317 3-terminal adjustable regulator



"**ACE**" — "**A**node **C**urrent **E**nters"

"**CCD**" — "**C**athode **C**urrent **D**eparts"

(Anode) + — (Cathode)

(d) Electrolytic capacitor

Figure A.1: Part pin-outs.

B Procedure: Measuring Line Regulation Characteristics

1. For the load L, **MAKE SURE** you use a $10\,\text{k}\Omega$ resistor at the output v_{out}.
2. ***COMPLETELY*** **DISCONNECT** v_{in} from **ALL** signal sources (**even sources that are off!!**).
3. Sweep v_{in} from 0–15 V in **ONE** of the following ways (but **NOT BOTH**!).
   (i) Use **function generator** with a *slow*[11] 0–15 V *triangle wave* (e.g., frequency $\approx 60\,\text{Hz}$, 7.5 V amplitude, 7.5 V offset). Do *not* generate a sawtooth wave!
   - **On old generators**, set *half* the desired offset (i.e., 3.75 V). Verify 0–15 V with scope.

   (ii) **AFTER connecting your oscilloscope in the NEXT step**, turn on `∞ Persist` under `Display` on your oscilloscope and *manually* swing the **power supply** from 0 V to 15 V.
4. Compare v_{in} and v_{out} using your oscilloscope's X–Y mode.
   (i) Connect v_{in} to channel 1 (i.e., X).
   (ii) Connect v_{out} to channel 2 (i.e., Y).
   (iii) Press the `Main` button in the `Horizontal` section of buttons at the top of your scope.
   (iv) Press the `XY` soft button on the screen to put the scope into X–Y mode.

   In this mode, at each instant of time, a single point is plotted with the channel 1 data as its X coordinate and the channel 2 data as its Y coordinate. Consider using `Averaging` under `Acquire`.

   Save this curve. **Use the cursors** to find the regulation region coordinates. **Record them.**
5. Let $v_{\text{in,min}}$ represent the minimum v_{in} that corresponds to a $v_{\text{out,min}}$ that is close to the nominal output (i.e., ∼4.3 V, ∼5.1 V, or ∼10 V). The *dropout (DO) voltage* is such that

   $$\text{Dropout Voltage} = v_{\text{in,min}} - v_{\text{out,min}}$$

   and has **units** of V; it is the minimum difference between input and *regulated* output (lower is better).
6. The region of v_{in} values with v_{out} close to the nominal output (i.e., ∼4.3 V, ∼5.1 V, or ∼10 V) is the *regulation region*. Let $v_{\text{in,left}}$ and $v_{\text{in,right}}$ be input values at the edges of this region (i.e., $v_{\text{in,left}} < v_{\text{in,right}}$), and let $v_{\text{out,left}}$ and $v_{\text{out,right}}$ be the corresponding output values.
   - *Line regulation (LR)* is most generally $\Delta V_{\text{out}}/\Delta V_{\text{in}}$. We care about two different versions:

     $$\text{LR (V/V)} = \frac{v_{\text{out,right}} - v_{\text{out,left}}}{v_{\text{in,right}} - v_{\text{in,left}}} \quad \text{and} \quad \text{LR (\%/V)} = \frac{v_{\text{out,right}} - v_{\text{out,left}}}{v_{\text{out,right}}} \times \frac{100\%}{v_{\text{in,right}} - v_{\text{in,left}}}$$

     where **units** are listed in parentheses. Different units may be used, but in all cases, lower is better.
     – Units of V/V (or μV/V) represent change in output under a 1 V change in input.
     – Units of %/V represent **percent** change in output under a 1 V change in input.
     – Units of % represent percent change in output voltage over entire range of rated input voltages.
     – Absolute units (e.g., mV) specify actual change over entire range of rated input voltages.

     Line regulation (and DO voltage) varies with load. Specification sheets will state the load used in testing. Some use a range or set of loads (e.g., full load, "typical" load, and no load).
   - The *power-supply-ripple-rejection (PSRR) ratio* is *approximately* so that

     $$\text{PSRR ratio} \approx 20 \log_{10} \frac{v_{\text{out,right}} - v_{\text{out,left}}}{v_{\text{in,right}} - v_{\text{in,left}}}$$

     and has units of dB. However, PSRR is an AC specification, and so this is a poor approximation. PSRR reflects the amount of input ripple power that passes through to the output. The PSRR should always be negative, and the more negative it is the better. Some specification sheets will omit the negative sign or include it in PSRR calculations; higher is better in these cases.

[11] Slow changes prevent excitation of hysteresis effects common in voltage references.

C Procedure: Measuring Load Regulation Characteristics

With a 15 V_{DC} input, apply several loads to find the regulator's *load regulation* and *quiescent current*.

- *Load regulation* characterizes how steady the regulator output is over a range of output currents.
- *Quiescent current* (QC) is the *additional* current required for operation (i.e., the "operating current").

Data collection tables (that you may *detach*) for each regulator are provided in Appendix D.

- Record data for each load in one of the rows of the table. You do not need to use the suggested loads, but you should choose loads close in value to the suggested ones.
- You may record data for the *no-load* (i.e., $\infty\,\Omega$, an *open* cicuit) case in the ∞ row of the table.
- For each load, there are *four* empty columns. Fill **two** with *measurements* and **two** with *calculations*.

Complete the following procedure.

1. ***COMPLETELY*** **DISCONNECT** v_{in} from **ALL** signal sources (**even sources that are off!!**).
2. Apply 15 V_{DC} to v_{in}.
3. Vary the load resistance from 0.02–10 kΩ either by:
   - picking **different discrete resistors**, or
   - using a **potentiometer** to swing through a range of resistances, or
   - using a **resistance block** to select different resistances.

   In Appendix D, **a table is provided for recording each regulator's data**. In each table, **some *suggested* loads are given**; you should choose *similar* loads based on what is available in the lab.

   For each resistance,

   (i) **measure and record (in table)** the
   - **output** v_{out} across the load (using DMM) and
   - **input current** i_{in} from the DC supply (using supply meter or ammeter *in series*), and

   (ii) **calculate** the
   - **output current** with $i_{out} = v_{out}/L$ and
   - **quiescent current (QC)** with $QC = i_{in} - i_{out}$.

   It is easiest to measure v_{out} using your **digital voltmeter (DVM)** (i.e., DMM on V_{DC} setting).

   CAUTION: For high loads (i.e., small resistances), the current may be large. To prevent your regulator from overheating,
   - turn the **power supply off between measurements**, and
   - **measure your v_{out} and i_{in} quickly.**

4. **Plot your load regulation data** with i_{out} on the horizontal axis and v_{out} on the vertical axis. There should be a region where v_{out} approximately matches the nominal output (i.e., ~4.3 V, ~5.1 V, or ~10 V) and the relationship between i_{out} and v_{out} is **approximately linear.** Use $v_{out,no\ load}$ and $v_{out,max\ load}$ to represent the v_{out} at the left and right of **this region**, respectively.

   Load regulation is most generally $\Delta V_{out}/\Delta I_{out}$. *Our* load regulation is such that

   $$\text{Load Regulation} = \frac{v_{out,no\ load} - v_{out,max\ load}}{v_{out,max\ load}} \times 100\%$$

   and has **units** of %. This load regulation, which is ideally zero, represents how steady the output will be across the entire range of rated loads. Other units (e.g., μV/mA or %/mA) give a measure of output change from under a unit load current change. Absolute units (e.g., mV) give output change over entire range of rated load currents. In all cases, lower is better. **Remember that load regulation only applies to the LINEAR regulation region** and **NOT to current limited regions.**

D Load Regulation Data Collection Tables

Use these tables to record the data from the procedure in Appendix C. Feel free to *tear them out* for easy access. There is one load regulation data table per regulator.

Zener Diode Voltage Reference

The schematic and procedure steps for this circuit are found in Section 1 on pages 2 and 3.

		Measurements		Post-lab Calculations	
Suggested Load (Ω)	Your Load (Ω)	v_{out} (V)	i_{in} (mA)	i_{out} (mA)	QC (mA)
∞	∞			0	
10 k					
6.8 k					
3.9 k					
2.2 k					
1.5 k					
1 k					
820					
680					
560					
470					
390					
220					
150					
100					
56					

Table D.1: Load regulation data for Zener diode voltage regulator/reference.

Current-Limited Discrete Transistor Adjustable Voltage Regulator

The schematic and procedure steps for this circuit are found in Section 4 on pages 7 and 8.

		Measurements		Post-lab Calculations	
Suggested Load (Ω)	Your Load (Ω)	v_{out} (V)	i_{in} (mA)	i_{out} (mA)	QC (mA)
∞	∞			0	
10 k					
6.8 k					
3.9 k					
2.2 k					
1.5 k					
1 k					
820					
680					
560					
470					
390					
220					
150					
100					
56					
22					

Table D.2: Load regulation data for discrete transistor adjustable voltage regulator with current limiting.

Discrete Transistor Adjustable Series Voltage Regulator with Current Foldback

The schematic and procedure steps for this circuit are found in Section 5 on pages 9 and 10.

		Measurements		Post-lab Calculations	
Suggested Load (Ω)	Your Load (Ω)	v_{out} (V)	i_{in} (mA)	i_{out} (mA)	QC (mA)
∞	∞			0	
10 k					
6.8 k					
3.9 k					
2.2 k					
1.5 k					
1 k					
820					
680					
560					
470					
390					
220					
150					
100					
56					
22					

Table D.3: Load regulation data for discrete transistor adjustable voltage regulator with current limiting.

LM317 Adjustable Positive Voltage Regulator

The schematic and procedure steps for this circuit are found in Section 6 on pages 11 and 12.

		Measurements		Post-lab Calculations	
Suggested Load (Ω)	Your Load (Ω)	v_{out} (V)	i_{in} (mA)	i_{out} (mA)	QC (mA)
∞	∞			0	
10 k					
6.8 k					
3.9 k					
2.2 k					
1.5 k					
1 k					
820					
680					
560					
470					
390					
220					
150					
100					
56					

Table D.4: Load regulation data for LM317 voltage regulator.